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VOICE OF THE ENGINEER

MARCH 6

Issue 5/2008

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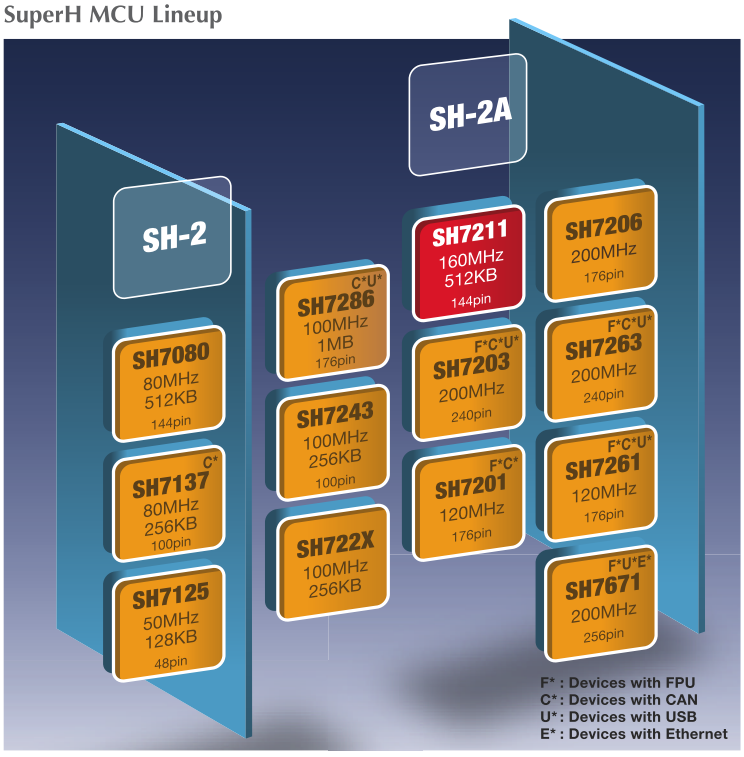
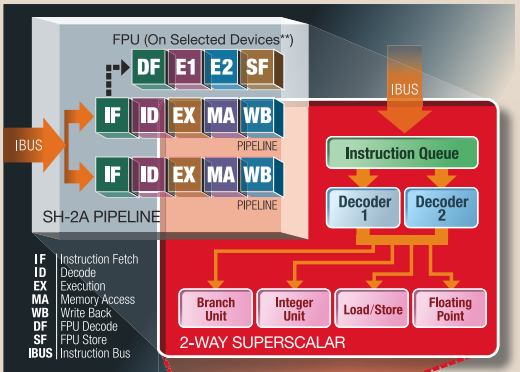
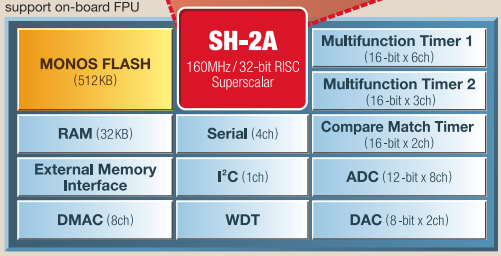
SuperH MCU Lineup



HOT Products **SH7211F**

(R5F72115D160FPV)





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*Source: Gartner (March 2007) "2006 Worldwide Microcontroller Vendor Revenue" GJ07168

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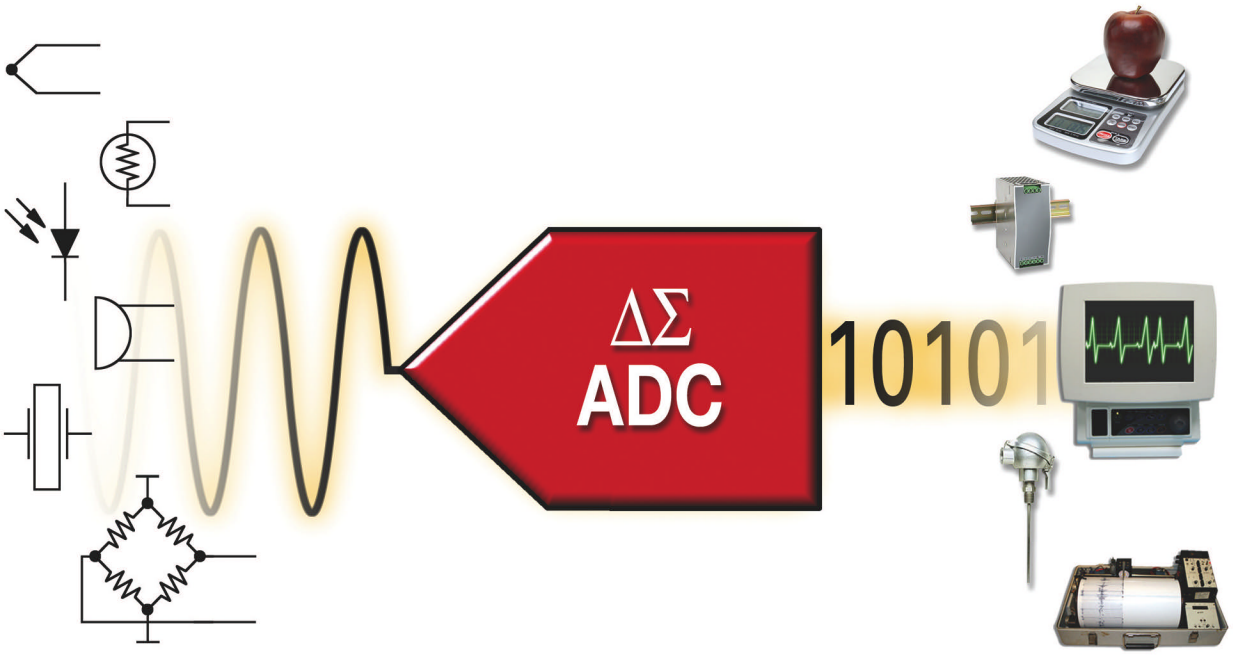

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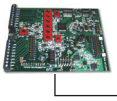

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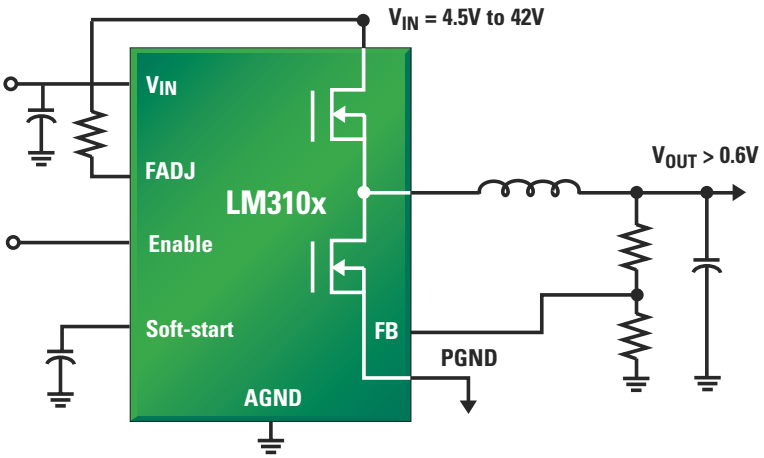

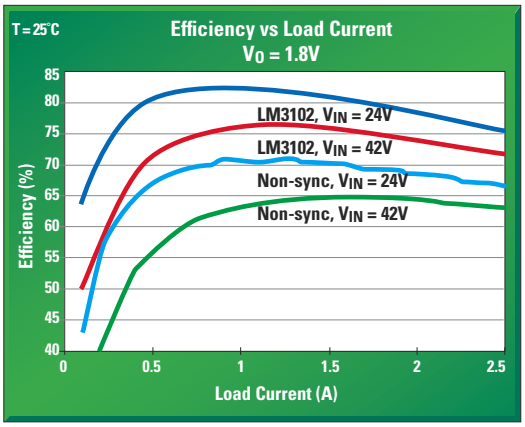

Product ID	V_{IN} Range (V)	Current (A)	V_{FB} (V)	Frequency (MHz)	Packaging
LM3100	4.5 to 36	1.5	0.8	Up to 1	eTSSOP-20
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Designing with QDRII+ and QDRII in one system

47 Although the latest QDRII+-SRAM devices offer speeds as much as 50% higher than QDRII products, a properly designed board can support either architecture.

by Jayasree Nayar, Cypress Semiconductor

Flyback transformer enables high power-factor and converter efficiency

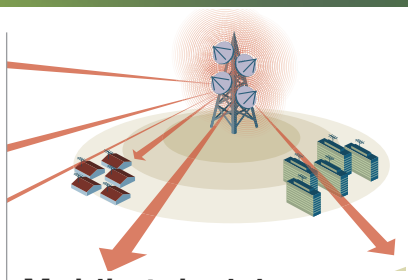
51 Ever-tightening regulations require a power factor of at least 0.9 and high efficiency for offline power supplies. This new switching-converter topology uses a flyback transformer and accomplishes both these goals in one stage.

by Cecil Deisch, Tellabs Operations Inc

Consumer ICs: designing for reliability

38 Consumers want the latest electronics but only if they'll last longer than the time it takes to take them out of their packages. IC vendors must tackle reliability issues so that their devices will find use in reliable, long-lasting products.

by Michael Santarini, Senior Editor

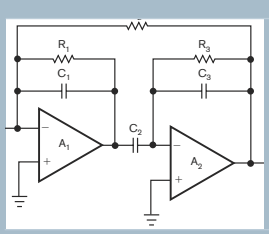


Mobile television: free—and location-free

29 If you think cellular's the only way you'll catch on-the-go television in the future, think again. Over-the-air broadcasters and satellite-based-service providers hope to catch the mobile-TV wave and ride it to fiscal success.

by Brian Dipert, Senior Technical Editor

DESIGNIDEAS



61 Audio equalizer features transimpedance Q-enhancement topology

66 AMI-to-NRZI-direct-conversion circuit tolerates unequalized pulse tails

70 Virtual RF generator measures load impedance and power

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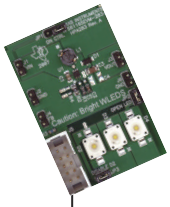

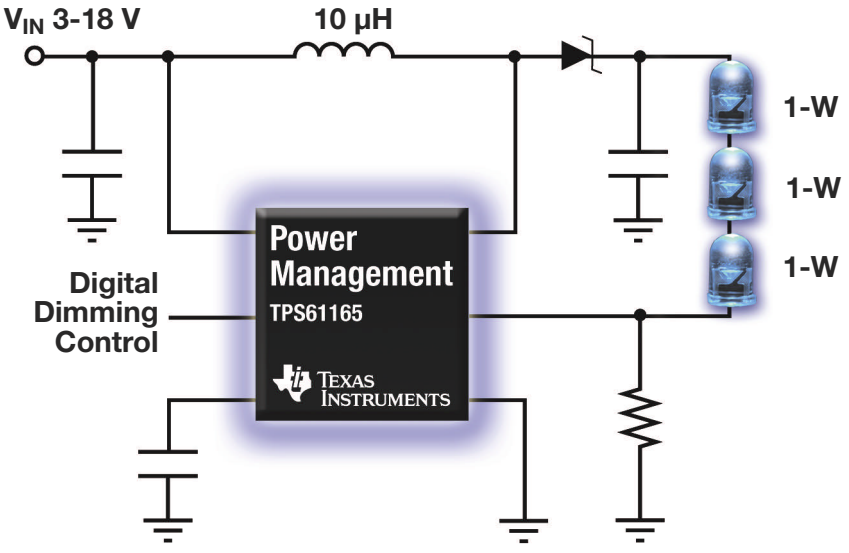

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TPS61165	Boost	10	3.0 to 18	1.2	38	90	2 x 2 QFN	$1.45
TPS61081	Boost	7	2.5 to 6	1.6	27	87	3 x 3 QFN	$1.45
TPS61150A	Boost	6 x 2	2.5 to 6	0.7	27	85	3 x 3 QFN	$1.65
TPS60251	Charge Pump	5 + 2 + 1	2.7 to 6.5	–	6.5	90	4 x 4 QFN	$1.40
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20 Network-media player drives multiple displays

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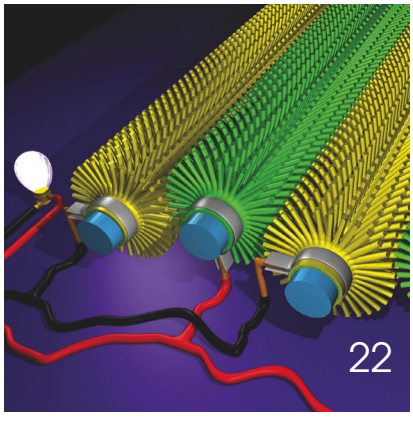

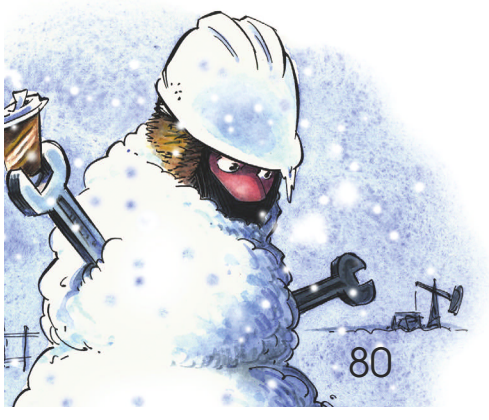

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PRODUCT ROUNDUP

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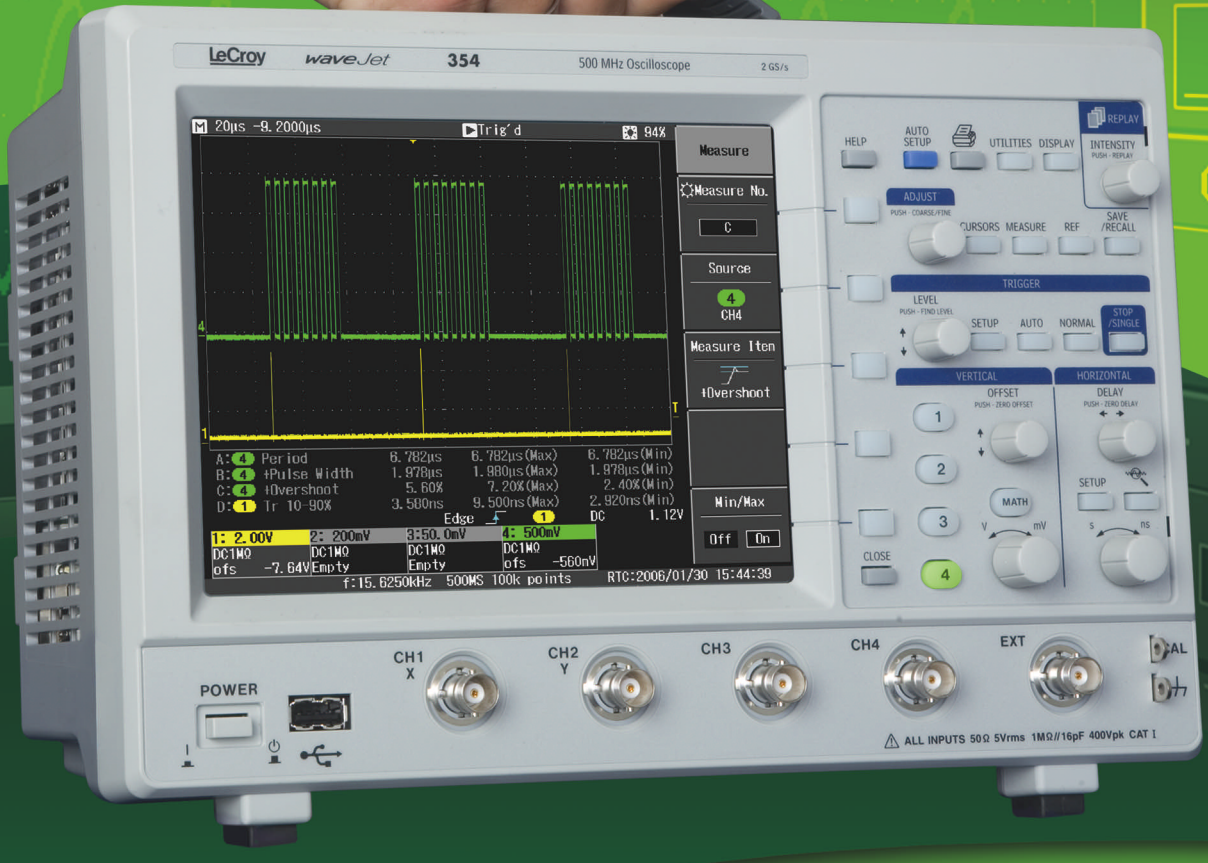

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READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

Mobile television: strong, weak, or zero reception?
On-the-go TV is here; some contend that it's been here for a while. Meanwhile, the number of "third-screen" options is rapidly expanding—from gear that fits into your palm to an LCD in the back seat of your car. But is anyone watching?
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Dealing with the devil: Could REACH be better than ROHS?
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Design an RTD interface with a spreadsheet
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Concerns arise about AMD Puma, analyst suggests AMD may soon be sold
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Intel, ST claim phase-change-memory prototypes
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MIT, TI develop proof-of-concept, energy-efficient microchip
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Intel accused of patent infringement in Core 2 Duo by Wisconsin tech transfer office
→www.edn.com/article/CA6530464

Intel, Micron claim world's fastest NAND flash
→www.edn.com/article/CA6527820

DISTRIBUTOR VIEWPOINT

As a companion to "Demand grows for distributor-demand creation" (pg 72), *EDN*'s Suzanne Deffree held a Q&A session with Harley Feldberg, president of Avnet Electronics Marketing. He sits in a unique position from which to assess how the economic slowdown impacts players across the electronics-supply chain.
→www.edn.com/article/CA6530480

FROM EDN'S BLOGS

There's lots of silicon in photovoltaic cells, but is there any gold for the electronics industry?

From *Practical Chip Design* by Ron Wilson

SEMI, always quick with the attractive luncheon topic, came up with a house-packing one recently: how electronics companies can make money from the current explosion of investment in solar energy generation.
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BY RICK NELSON, EDITOR-IN-CHIEF

Fractal engineering versus synergy

Engineering is a segmented profession. It divides into high-level disciplines—mechanical, electrical, civil, chemical, structural, automotive, aerospace, and so on. When you look closely at these high-level disciplines and begin to break them down, you find—fractal-like—that you don't make much headway in reducing the number of areas of engineering specialization available. Just as a fractal divides and repeatedly subdivides into components that appear to be as complex as the original, engineering disciplines divide and repeatedly subdivide into specialties of increasingly fine yet no less complex granularity.

Take electrical engineering, for example. It breaks down into application segments such as power, communications, consumer electronics, avionics, computers, software, telematics, and medical electronics. For each application area, you can subdivide further into ICs, PCBs (printed-circuit boards), subassemblies, subsystems, and systems. Further, each discipline offers a choice of specialties focusing on R&D, validation, debugging, characterization, production, field installation and repair, and so on.

This segmentation is appropriate. Engineering is too complex for any practitioner to become proficient in more than a few specialization areas, and it's necessary to rely on teams comprising specialists to cover all the facets necessary to get a product to market. Despite the emergence of ESL (electronic-system-level) design, it's difficult for RTL (register-transfer-level) designers, for example, to grasp all the complexities of the aerospace, medical, or automotive products that the ICs they are designing might ultimately populate.

Unfortunately, specialization often results in the formation of walls. The classic wall separates design and test, but, even within test, walls arise that are counterproductive to the cost-effective production of quality products. In the March issue of sibling publication *Test & Measurement World*, I report on a wall that arises between two test disciplines. In that article, Glenn Woppman, president and chief executive officer of Asset InterTech, commented on his company's acquisition of International Test Technologies: "We've found another wall—[we hope] not as high a wall—between structural test and functional test," he says.

Breaking down the walls between design and test and those between the various test subsets requires a holistic approach toward our subject matter. And holistic approaches, such as the Semiconductor Test Consortium's STIX (Semiconductor Test Interface Extensions) initiative, do exist. The initiative addresses the rising cost and efficiency challenges that impact ATE (automated test equipment), such as enabling greater portability of test collateral through higher level abstraction of user programming, equipment integration, and device interconnect. "[STIX] dramatically increases the potential positive impact of the consortium on the semiconductor industry by extending its influence beyond simply the tester architecture," stated Steve Wigley of the Semiconductor Test Consortium and LTX, writing on www.tmworld.com. "It represents a more holistic approach to addressing the technical and economic issues that affect the entire global-semiconductor-test-supply chain."

Meanwhile, Jack Erickson of Cadence Design Systems addressed power closure, writing in *EDN* that it is "important to address this issue as early and as holistically as possible. The most efficient way is with a central specification of the power-implementation architecture that allows a single change to propagate across the flow. At the end of this exercise, you will have a good idea of the power consumption, timing feasibility, physical feasibility, and functional correctness."

The bottom line is that holistic is good, but even the best efforts of today bring together only the most closely related fractal components of the electrical-engineering profession. And that statement brings up why I'm writing this editorial. I've been writing and reporting for nearly 10 years for *Test & Measurement World*, most recently serving as Editor-in-Chief. I'll retain that position while also taking on the responsibilities of *EDN*'s Editor-in-Chief. In that role, I'm rejoining the magazine in which I got my start in technical journalism after leaving the engineering profession. The respective *EDN* and *TMW* staffs will continue their focus on their specialties but will also concentrate on the synergetic intersections of their respective areas of expertise to bring you the information you need to succeed in this multifaceted world. EDN

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ANALOG edge[SM]

Power Supply Design Techniques for FPGAs

Application Note AN-1677

Tim Hegarty, Applications Engineer

The Xilinx Virtex™-5 and Altera Stratix® III are families of advanced FPGAs based on 65-nm cores that combine various platforms and speed grades enabling a high level of performance and flexibility. This article discusses FPGA power supply prerequisites as needed by the system designer in terms of the multiple voltage rail and current level requirements, output sequencing, and startup characteristics. Following, a power supply solution based on National Semiconductor's LM1771 and LM3880 is designed that combines high performance, power density and efficiency.

FPGA Power Supply Requirements

The Virtex-5 or Stratix III FPGAs generally require at least two different voltage rails. The recommended Virtex-5 core voltage, designated V_{CCINT}, is 1.0V±50 mV while the Stratix III core rail, denoted V_{CCL}, can be selected as 0.9V±40 mV or 1.1V±50 mV. Depending on the I/O standard being implemented, the Virtex-5 I/O voltage supply, V_{CCO}, can vary from 1.14V to 3.45V. Thus, V_{CCO} voltage rails of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V are feasible. Similarly, Stratix III specifies that the I/O voltage, V_{CCIO}, can vary from 1.14V to 3.15V, yielding 1.2V, 1.5V, 1.8V, 2.5V, and 3.0V as voltage rail possibilities.

Furthermore, Xilinx defines an auxiliary voltage, V_{CCAUX}, which is recommended to operate at 2.5V±5% to supply FPGA clock resources. Altera defines additional rails specified for the digital and analog PLL sections, I/O pre-drivers, differential clock inputs, and such. It is required that the power supplies transiently handle larger currents during startup with relatively lower static and dynamic currents during normal operation. The power-up ramp time specification for each voltage rail is 0.2 ms to 50.0 ms for the Virtex-5 and 0.1 ms to 100.0 ms for the Stratix III.

FPGA Power Supply Design Outline

This proposed FPGA power supply solution is aimed at the Virtex-5 FPGA. A corresponding power supply strategy can be implemented for the Stratix III with subtle changes considering the aforementioned differences.

The power-on sequence recommended by Xilinx is V_{CCINT}, V_{CCAUX}, and V_{CCO}. Although any monotonic power-on sequence is tolerated, use of the recommended sequence allows Xilinx to define the minimum inrush current required from the FPGA core, auxiliary and I/O supplies - denoted $I_{CCINTMIN}$, I_{AUXMIN}, and I_{CCOMIN}, respectively - to ensure correct power-on and configuration. The solution uses three National Semiconductor LM1771 PWM controllers with power-up and power-down of the individual voltage rails sequenced by a National Semiconductor LM3880 power sequencer.

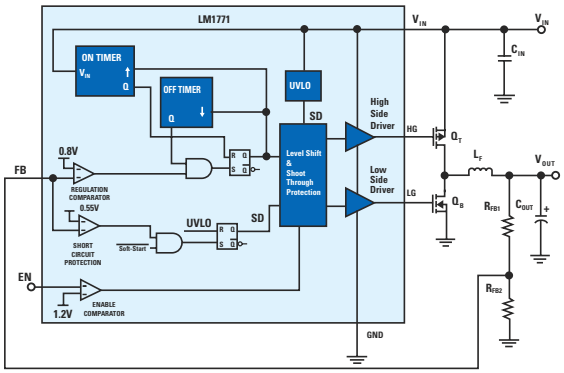

Figure 1. LM1771 DC-DC Buck Stage with COT Control Architecture

The LM1771 block diagram with typical external components is presented in ***Figure 1***. The LM1771 is an efficient buck converter switching controller available in MSOP-8 and LLP-6 packages and capable of converting an input voltage between 2.8V and 5.5V into a regulated output voltage as low as 0.8V. It drives an external high side PFET and low side NFET and utilizes a constant on-time (COT) control architecture which eliminates the need for an error amplifier and external compensation components. Thus, extremely fast transient load current response is possible. Additionally, the LM1771 features a precision enable pin to facilitate supply sequencing and/or flexibility in setting the operating range of the power supply.

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Three LM1771 timing options - designated S, T and U in the part numbering specification - are available which translate to three possible frequency options for a given output voltage. For a given timing option, the switching frequency is independent of input voltage level as the controller input feed-forward feature varies high side switch on-time as a function of input voltage to maintain constant volt-seconds at the switch node.

By virtue of the small-sized package options, the LM1771 allows for a complete power supply design to occupy very little PCB real estate without sacrificing efficiency or performance.

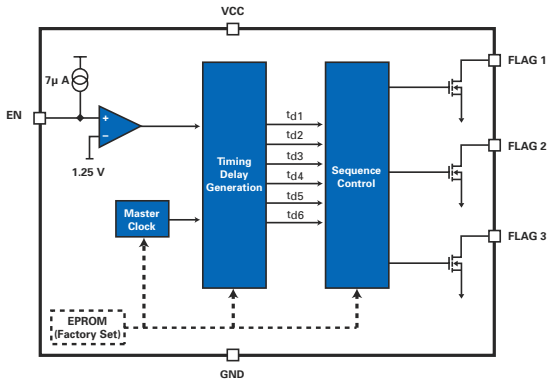

Figure 2. LM3880 Sequencer Block Diagram

The LM3880 sequencer block diagram is presented in ***Figure 2***. It is available in a SOT23-6 package and it has three open-drain flag outputs which allow control of the three LM1771 enable pins. Upon enabling the LM3880, the three output flags will sequentially release, after individual time delays, permitting the connected power supplies to startup. The output flags will follow a reverse sequence during power down to avoid latch-up conditions. Standard timing options of 10 ms, 30 ms, 60 ms and 120 ms are available. Additionally, the LM3880 is factory programmable to attain customized timing options combined with six possible power down sequences.

FPGA Power Supply Implementation

The LM1771 and LM3880 based power train schematic is shown in ***Figure 3***. For this design, the three buck regulator channels are capable of delivering maximum continuous load currents of 5A, 3A and 3A (I_{CCO}, I_{CCAUX}, and I_{CCINT}, respectively). The I/O voltage is set at 3.3V, but can be easily varied by modifying one of the feedback resistors. The core and auxiliary rails are set at 1.0V and 2.5V, respectively.

The core, auxiliary and I/O regulators use the LM1771S, LM1771T and LM1771U controllers which yield switching frequencies of 606 kHz, 758 kHz and 500 kHz, respectively. Each supply has its own input filter capacitor located as close as possible to the p-channel and n-channel buck and synchronous power FETs. Additionally, a small input bypass capacitor is placed local to each LM1771 IC.

The output filter capacitances on the core and I/O supplies are tantalum based and chosen to present the necessary Equivalent Series Resistance (ESR) to maintain sufficient in-phase ripple at the Feedback (FB) pin. A feed-forward capacitor from V_{CCO} to the FB pin increases the magnitude of the ripple seen by the LM1771. The output filter capacitance of the auxiliary voltage regulator is ceramic based to minimize the noise level of this rail. A resistor capacitor current sense network across that channel's filter inductor creates a triangular waveform which is ac coupled to the FB node. This circuit can also be utilized in the core and I/O channels if tantalum capacitors are deemed unsuitable and/or low ESR ceramic capacitors are required either local to the regulator or downstream adjacent to the FPGA.

The filter inductors are designed for large current handling capability with low DC and AC effective resistance to maximize efficiency. The inductance value is conditioned to attain peak-to-peak ripple current of approximately 30% of the rated load current. Further, it is desirable to choose a relatively soft saturation characteristic to handle short duration high current transient events in excess of the rated load current.

TSOP-6 packages are used for the power FETs in the auxiliary rail supply while SO-8 FETs are implemented for the I/O channel regulator. The core voltage supply, given its low duty cycle operating point, has a high side TSOP-6 FET and a low side SO-8 FET.

The LM3880 30 ms timing option, designated -1AB, is recommended. External pull-up resistors are connected to each open-drain flag output.

To read the complete article, visit:
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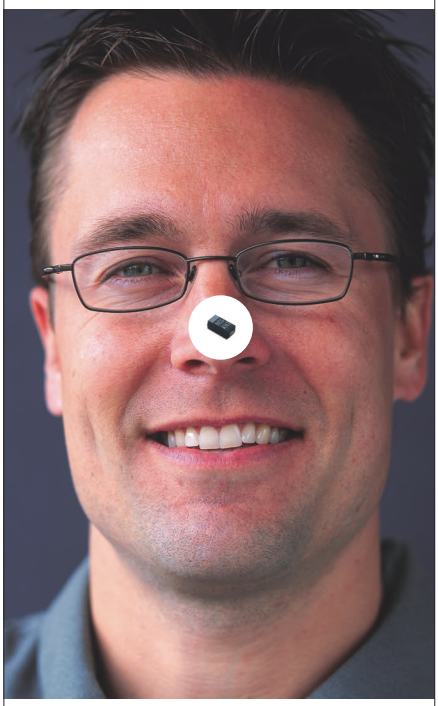

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Logic-analyzer-based instruments debug, validate MIPI physical layer

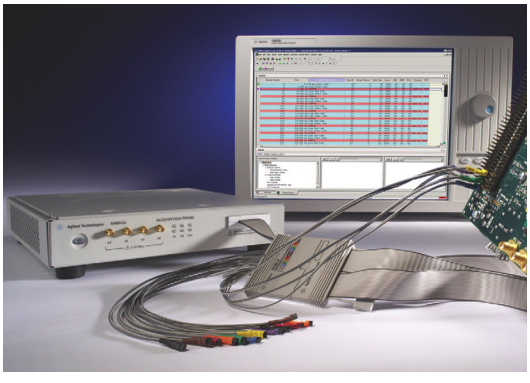
Agilent Technologies believes that verifying, debugging, and establishing D-PHY (500-Mbps-physical-layer)-based products' specification conformance and interoperability requires specialized tools and that the logic analyzer is the correct platform on which to base such tools. Logic analyzers may at first seem a curious choice because they work with slow and wide parallel buses rather than with fast and relatively narrow serial buses, such as D-PHY. However, serialization and deserialization readily adapt logic analyzers to the higher-speed serial topology. More important, when you use logic analyzers with the appropriate software, they are the most appropriate instruments for displaying packet data in a manner that allows developers to quickly uncover the causes of device-under-test malfunctions.

The MIPI (mobile-industry processor-interface) Alliance's (www.mipi.org) high-speed, low-pin-count, low-power serial-interconnect D-PHY standard originally intended to target a maximum data rate of 500 Mbps per lane. (The D in the acronym is the Roman numeral for 500.) However, the bus is capable of twice that speed: 1 Gbps per lane. Mobile devices—cell phones, cameras, music players, handheld TVs, and the like—represent a huge market for D-PHY, perhaps exceeding a billion units per year.

D-PHY's difficult-to-achieve combination of low cost, low power, high data rate, and compact size bode well for its use in many other types of electronic devices, as well. Implementing D-PHY may, however, prove somewhat more demanding than implementing other high-speed serial protocols: Visibility of some signals can present challenges, and D-PHY lanes are inherently half-duplex to minimize pin count, whereas most other popular high-speed serial standards are full-duplex. You can use two D-PHY lanes to implement full-duplex communication or, if the data rate is amenable, you can reverse a half-duplex lane's transmission direction on the fly.

Agilent's D-PHY product-test offering comprises the N4851A analysis probe with a US list price starting at $13,561 and the N4861A stimulus probe with a price starting at $14,566. You use both units with the company's 16900A logic analyzer. Your 16900A should include one or more plug-ins having at least 68 channels. Agilent expects large numbers of developers to require the analysis probe, whereas fewer will require the stimulus probe, which enables the logic analyzer to simulate D-PHY-based hardware. Software that accompanies the probes resides in the 16900A, enabling it to generate D-PHY-specific displays. Both instruments and the accompanying software support the MIPI Alliance's CSI-2 (camera-serial-interface) and DSI (display-serial-interface) D-PHY-based protocols for mobile devices.**—by Dan Strassberg**

▷**Agilent Technologies**, www.agilent.com/find/mipi.



The N4851A analysis probe handles deserialization of the MIPI D-PHY 1-Gbps-per-lane physical-layer signals so that the 16900A logic analyzer with one or more plug-ins having at least 68 channels can display the data frames in a manner that reveals the causes of transmission errors.

FEEDBACK LOOP

"Once again, the authors do a superb job of describing and evaluating the battery-stack-voltage-monitoring issues that I currently have to deal with in my high-volume-lithium-ion-automotive application."

—Reader David Kapolka, praises a feature article, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6515356. Add your comments.

Magma offers DRC-incremental Talus

Magma Design Automation has introduced the Talus QDRC (Quartz design-rule-checking) tool to help designers with the placement and routing of ICs. Designers traditionally run DRC after detailed routing to ensure that their designs do not violate any of the targeted foundries' process rules. If they find mistakes, they must transfer the GDSII (Graphic Design System II) files back to place-and-route tools to fix them. After they implement those corrections, the designers often introduce new violations, so they must repeat the process. Streaming the GDSII files between tools can take several hours or even days. A typical design with 10 million instances turns into an approximately 8-Gbyte GDSII file.

Magma hopes to ease and speed the process with the new tool, essentially an integrated DRC within the implementation flow operating on Magma's unified data model. "The major advantage is that you can now do DRC on the implementation database and eliminate the need to stream GDSII into DRC tools to make the changes," says Kevin Walsh, senior vice president of marketing for Magma's physical-verification-business unit. The designs are getting so large that streaming out the files affects data integrity, and you pay the cost of the stream-out time and the time it takes to correct a violation so that you can move on to the next step in the flow. QDRC allows users to do some DRC at the point during which the violations are most likely to occur, which saves stream-out, analysis, and at sign-off time. Because QDRC operates on Magma's memory-resident data model, it allows you to do a true incremental DRC, says Walsh.

> "Using the tool will allow users to cut overall DRC time from days to hours.

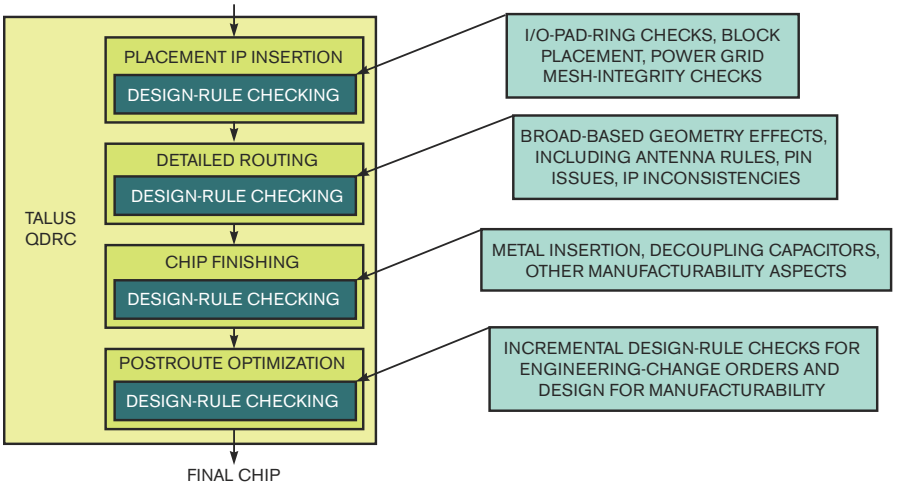
Other vendors claim to also have incremental-DRC tools, but Walsh says that competing tools stream out large GDSII files and then generate reports on different parts of the design so users can get to work on those problems. After designers do placement and IP (intellectual-property) insertion, for example, they can run QDRC to do I/O-pad-ring checks, block placement, and power-grid-mesh-integrity checks. After detailed routing, they can do broad-based geometry effects, including antenna rules, pin issues, and IP inconsistencies.

At the chip-finishing stage, they can run checks for metal insertion, decoupling capacitors, and manufacturability aspects. During postroute optimization, they can run incremental DRC for engineering change orders and DFM (design for manufacturability). They can then run the final GDSII files through sign-off DRC using DRC tool, Mentor's (www.mentor.com) Calibre, or a similar tool.

QDRC notes whatever the placer or the router has changed and then checks only those parts of the design. "It allows you to preserve data integrity and efficiency of the operation," says Walsh. Magma claims that using the tool in SOC (system-on-chip) flows will allow users to cut overall DRC time from eight days to roughly 20 hours, that performance is linearly scalable, and that it can run in a small memory footprint. QDRC's prices vary, depending on options, but a stand-alone version sells for $40,000 to $60,000.

—by Michael Santarini

▷**Magma Design Automation**, www.magma-da.com.



The Talus QDRC (Quartz design-rule-checking) tool helps designers place and route ICs.

DILBERT By Scott Adams

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Open Verification Methodology is ready for download from Cadence, Mentor

Semiconductor-design-software companies Cadence Design Systems Inc and Mentor Graphics Corp recently announced that their jointly developed OVM (Open Verification Methodology) source code, documentation, and use examples are now ready for free downloading from www.OVMWorld.org. The companies distribute OVM under the standard open-source Apache 2.0 license from the OVM Web site, which is the central point of access for the OVM source code, providing information about partners, events, seminars, training, how-to instructions, and future plans.

Cadence and Mentor based OVM on the IEEE Standard 1800-2005 SystemVerilog standard. OVM is the first open-language-interoperable, SystemVerilog verification methodology. It comprises a methodology and accompanying library to allow users to create modular, reusable verification environments in which components communicate with each other through standard transaction-level modeling interfaces.

The OVM also allows intra-company and intercompany reuse through a common methodology and classes for virtual sequences and block-to-system reuse and full integration with other languages that production flows commonly use. Multiple verification platforms support OVM. These platforms suit both novice and expert verification engineers. OVM includes the foundation-level utilities for building advanced object-oriented, coverage-driven verification environments and reusable VIP (verification intellectual property) in SystemVerilog. OVM also reduces the complexity of adopting SystemVerilog by embedding verification practices into its methodology and library, and it reduces the time it takes to create verification environments by integrating plug-and-play VIP and ensuring code portability and reuse.

Robert Hum, vice president and general manager of Mentor's verification-and-test-business unit, notes that OVM represents a major step in protecting customers' investment in verification flows and reusable VIP. Mentor believes that OVM will accelerate the move to SystemVerilog, and provide significant competitive advantages to design-and-verification teams.

A production version of OVM is available now, and the companies plan to add functions this year. Both companies have ensured that the OVM runs on their simulators and allows backward compatibility with their previous environments: Mentor's Advanced Verification Methodology and Cadence's Incisive plan-to-closure methodology.

—by Ann Steffora Mutschler

▷**Cadence Design Systems Inc**, www.cadence.com.

▷**Mentor Graphics**, www.mentor.com.

NETWORK-MEDIA PLAYER DRIVES MULTIPLE DISPLAYS

Video displays showing advertising-laden content are popping up in strategic locations, such as gas stations, supermarkets, fast-food dining areas, and airport waiting areas.

One company in this market, Apollo Display Technologies, manufactures many of the electronic systems driving these displays, including the recently released ArtistaMedia single-board network-media player.

The ArtistaMedia network-media controller plays stored or streaming video on flat-panel displays at high-definition resolutions as high as 1080p.

The board includes a TFT (thin-film-transistor)-LCD controller for playback of videos from a CompactFlash card, 2.5-in. hard-disk drive, or streaming server. You can load or update your stored MPEG-2 or MPEG-4 videos using Ethernet, a CompactFlash card, or a USB stick and play them back in a continuous loop on an unlimited number of displays. Playback is also possible from a streaming-video server without local storage.

ArtistaMedia features onboard audio support and display resolutions of 640×480 pixels to full high-definition 1080p. The board allows direct Ethernet connection of TFT LCDs and eliminates the need for a client PC and operating system at each display. If you don't have or want a network, you can operate ArtistaMedia as a stand-alone player from the supplied CompactFlash card or an optional hard disk.

Other options include an onboard touch controller, a keypad interface, and remote control. The ArtistaMedia player and application software sell for less than $300 (1000). Delivery is in four to six weeks.

–by Warren Webb

▶Apollo Display Technologies Corp, www.apollodisplays.com.

03.06.08

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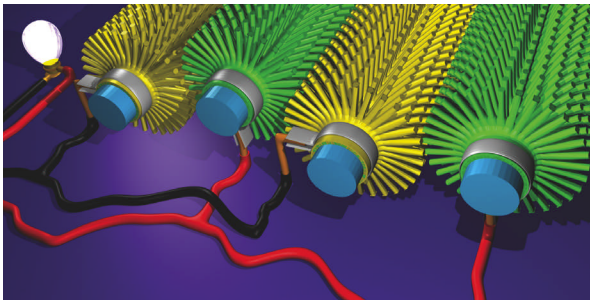
ANALOG DEVICES

RESEARCH UPDATE

BY MATTHEW MILLER

Fiber-based energy harvester potentially turns garments into generators



Researchers sewed nanowire-encrusted fibers into garments. When someone jostles the garment, the wires produce electricity.

Researchers at the Georgia Institute of Technology have developed a textile-based generator that could enable garments to convert the wearer's movement into electricity to power personal electronic devices. The researchers coax billions of zinc-oxide nanowires to grow radially from a Kevlar fiber, yielding a structure they liken to a bottle brush.

A generator features two such fibers arranged in parallel. One of the fibers gets an additional coating of gold that allows it to serve as the electrode. Employing the same basic principles as an earlier harvester, the generator creates electrical energy via the piezoelectric effect when movement causes the two fibers to rub together (see "Energy harvester generates continuous nanoampere current," *EDN*, May 24, 2007, pg 28, www.edn.com/article/CA6442450).

The researchers have measured 4 nA of current and 4 mV of output voltage from a generator employing 1-cm fibers. They estimate that, with design improvements, a square meter of fabric should be able to generate 80 mW. One major barrier to commercialization remains, the team admits: Zinc-oxide is vulnerable to water, so the technology still needs a mechanism for washing-machine survival.

▷**Georgia Institute of Technology**, www.gatech.edu.

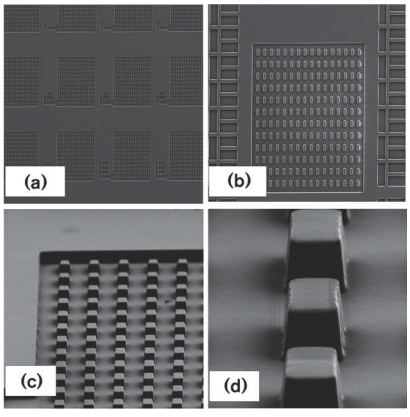
Cool-curing polymer simplifies IC fabrication

Rensselaer Polytechnic Institute and Polyset have developed an inexpensive, quick-drying polymer that promises to cut costs for current IC-packaging processes by simplifying the construction of redistribution layers. Meanwhile, the material also shows promise in ultraviolet on-chip nanoimprinting lithography, a potential next-generation IC-patterning technology.

The material, PES (polyset-epoxy siloxane), cures at 165°C, about 35% cooler than the benzocyclobutene and polyimide that chip-packaging companies now rely on for redistribution layers. That reduced need for heat translates directly to savings in overhead costs, according to the researchers. The material matches the other materials in key characteristics, such as thermal stability, low thermal expansion, low dielectric constant, and low leakage current, but surpasses them in water-uptake rate and the ability to adhere to copper.

▷**Rensselaer Polytechnic Institute**, www.rpi.edu.

▷**Polyset**, www.polyset.com.



A series of electron-microscope images of a new polymer at 30 microns (a), 10 microns (b), 3 microns (c), and 1 micron (d) show its ability to create well-defined patterns in a UV-imprint-lithography application.

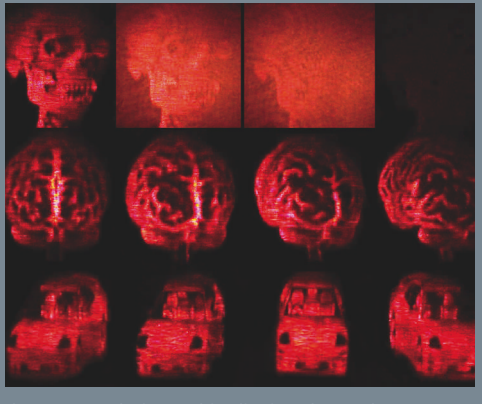
03.06.08

HOLOGRAPHIC DISPLAY HAS A REFRESH RATE OF MINUTES

Scientists at the University of Arizona have developed what they claim is the first updatable, 3-D holographic display. Viewable without special eyewear, the 4×4-in. prototype features a photorefractive polymer between two pieces of electrode-coated glass. The system writes images onto the light-sensitive polymer using laser pulses and an externally applied electric field. The display can produce a new image in about three minutes.

With medical applications in mind, the researchers hope to produce displays as large as 3×3 feet and produce full-color holographic images.

▶University of Arizona, www.arizona.edu.



A prototype holographic display shows the erasing process (top row) and 3-D perspective (bottom two rows), which could prove invaluable in military and medical applications.

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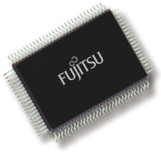

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BY HOWARD JOHNSON, PhD

Z_{MIN}, a very special value

The driver in **Figure 1** precisely meets its specified high- and low-output-voltage levels with a termination resistance of 25Ω. If you increase the resistor's value, the circuit becomes progressively easier to drive, making the waveform exceed the specs in both directions. If you decrease it, the driver fails to produce a sufficiently large signal.

Resistor R_T controls the gain of the circuit, and the termination voltage controls the dc offset. Between gain and offset, you have everything you need to effect complete control over the output waveform, within reason.

When you design an end-terminating circuit, you must select an effective termination resistance large enough to guarantee that the driver can produce a full-sized output swing and then set the effective termination voltage to center the waveform so it crosses both the high- and the low-output voltages. No matter what topology you use to implement the final circuit, whether it looks like a resistor-and-battery arrangement or a voltage-divider (split-terminator) structure, the gain and offset constraints apply.

The smallest value termination resistance for which the output swing can, with a perfect setting of termination voltage, just barely touch both the high- and the low-output voltages, with no tolerance for error and no margin, is a very special value I call Z_{MIN} (minimum impedance). Understanding this value is the secret to successful end-termination design.

The value of the minimum termination impedance derives from a general output-current relation. Simply, the driver output current always equals the voltage drop across the resistor divided by its value in ohms. If you correctly set the minimum impedance, then, when the driver pulls high to the high-output voltage, the current precisely equals the high output current:

$$I_{OH}=(V_{OH}-V_T)/Z_{MIN}, \quad (1)$$

where I_{OH} is the high output current, V_{OH} is the high output voltage, V_T is the termination voltage, and Z_{MIN} is the minimum impedance.

In the low state, you get a similar relationship:

$$I_{OL}=(V_{OL}-V_T)/Z_{MIN}. \quad (2)$$

Subtract **Equation 2** from **Equation 1**:

$$I_{OH}-I_{OL}=(V_{OH}-V_{OL})/Z_{MIN}. \quad (3)$$

Solving for Z_{MIN} yields the "golden" equation of end-termination design:

$$Z_{MIN}=(V_{OH}-V_{OL})/(I_{OH}-I_{OL}). \quad (4)$$

Equation 4 says that the minimum impedance equals the spread in voltage between the high-output voltage and the low-output voltage divided by the spread in current between the high-output current and the low-output current. Your driver can never successfully drive any load with a long-term impedance of less than the minimum impedance.

When working **Equation 4**, pay attention to the polarity of the currents. Source current is positive. Sinking current is negative. For example, if a driver sources and sinks 25 mA, then its spread is (25−(−25))=50 mA.

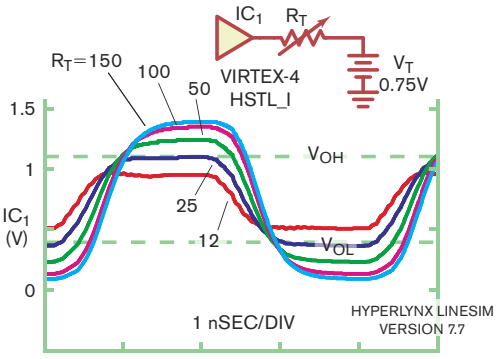

Figure 1 Reducing the value of R_T shrinks the output voltages.

Suppose that the minimum impedance for your driver works out to 60Ω. I would not use an end termination with that value. It leaves no room for component tolerance. Other effects, such as temperature and age variation in the termination voltage, can knock the circuit out of specification. You should use a slightly larger value, such as 70Ω.

On a 50Ω transmission line, a 70Ω termination won't be perfect. It will cause a reflection of (70−50)/(70+50)=16.7%. If that's too much for your voltage-margin budget, then consider raising the transmission-line impedance. Bring the line impedance up to perhaps 60 or 70Ω. The closer you bring the transmission-line impedance to the termination resistance, the better your system will work.

The optimal value for the termination resistance is just a little higher than the minimum impedance to account for tolerances, with a transmission-line impedance as close as practical to the termination resistance. EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Know your IP provider

With the shortened time to market for consumer and industrial products and the rapid introduction of new process technologies through the foundry market, there is a rash of new IP (intellectual-property) companies offering substandard and misrepresented products. The trend was inevitable in a growing marketplace. However, the presence of weak IP companies impacts the viability of the properly engineered and supported IP companies. Additionally, countless chips and end products will fail to work, have reliability issues, and be difficult to debug as a result of these substandard IP blocks.

The selection of the IP provider and the blocks and functions involved is *not* just a business issue. Although business aspects are always important, for IP modules built in less-than-130-nm processes, the validation of the IP and the infrastructure supporting it are key criteria. Just how important? Currently, one of the largest causes of SOC (system-on-chip) failures from foundry shuttle runs or prototype runs is the use of unqualified IP in the design.

Every SOC builder's checklist should include some IP-provider selection criteria. First, does the company have legitimate licenses for the EDA tools it is providing kits for? Many companies are outsourcing major portions of the design to Eastern Europe, India, and China, where software piracy is very visible. Pirated software tends to lack the current patches or the metadata that make it compatible with current legitimate code and could result in noncorrectable problems in design-for-manufacturing and mask-data-preparation steps.

It is the norm in the current global design community for the development site to be separate from the point of sale.

Second, does the company have a history of commercially manufacturing the IP or parts? A number of companies are promoting silicon-proven experience when the only actual silicon they have run has been government-funded or -subsidized test chips on Defense Department or university processes. In most cases, the IP that a company sends to a fab on an MPW (multiproject wafer) under a military contract is not releasable to others because of licensing issues. In these cases, the vendor claiming silicon-tested IP is actually sending modified, process-migrated, and untested IP to its commercial customers—only "validated" by these other, different designs.

Third, does the company's engineering team have the experience and support level you need? The larger IP providers, such as ARM, Synopsys, and Mentor, all have standard documented application and design support for their IP that includes device and RTL integration, tool integration, application verification, physical implementation and verification, and test development. The smaller IP providers are sometimes staffed only by recent university graduates and a research support team that cannot support the IP in a context of an SOC, because they have little to no real chip-building or CAD-tool-flow experience.

Fourth, does the company have the designers of its IP in-house? One of the basic assumptions is that the IP provider you are dealing with actually created the block you are licensing. In reality, some IP companies are merely brokering blocks that contractors created, IP it acquired from other companies, or blocks that are process migrations from pirated IP libraries that are floating around the industry.

This repackaging is difficult to identify at the data level and requires finding an IP company that will identify the location of its design group and offer an avenue for the end licensee to reach this group to modify or integrate the IP block in its SOC design. In this context, in-house does not necessarily mean the same location; it is the norm in the current global design community for the development site to be separate from the point of sale. However, the designers should be accessible—not moonlighting engineers in import- or export-restricted countries.

Look for additional guidelines and physical-design keys in a future article. EDN

Contact me at pallabc@siliconmap.net.

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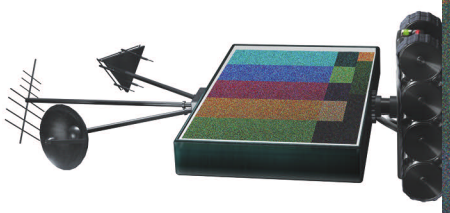
BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR



MOBILE TELEVISION: FREE—AND LOCATION-FREE

PART 2

EDN's recent mobile-television article focused mostly on transmission protocols amenable—for technical reasons, business reasons, or both—to cellular handsets, including DVB-H (digital-video-broadcasting-handheld), EVDO (evolution-data optimized), UMTS (universal-mobile-telecommunications system), and MediaFlo (**Reference 1**). However, as Japan's 1seg and South Korea's T-DMB (terrestrial-digital-multimedia-broadcasting) networks suggest, it's possible to graft support for conventional digital-television broadcasts onto a mobile phone if the economics justify the surgery. And, as the earlier article points out, it's not a foregone conclusion that the cellular handset will be the predominant means by which viewers tune into mobile TV (see **sidebar** "More ahead").

Any secondary application that drains the battery and precludes subsequent access to the unit's primary application—making and taking telephone calls, for example—will likely receive a cool reception by consumers, especially if it's also one that considerably adds to the unit's price tag. Mobile TV has both qualities. A significant disparity between all-in-one widget aspirations and feasible reality opens the door to system alternatives with more focused functions and to a lengthier list of alternative infrastructure approaches.

A NETWORK COUNTERATTACK

Before last month's 3GSM (Third Generation Groupe Spéciale Mobile) Congress conference in Barcelona, Spain, Michael Rayfield, handheld-business-unit general manager at Nvidia, agreed—at least from a technical standpoint—with what the material in **Refer-**

ence 1 points out: that generational improvements in DVB-T's (digital-video-broadcasting-terrestrial) power-consumption characteristics might obviate the need for a late-arriving DVB-H descendant. However, from a business perspective, subscription-supported cellular carriers control DVB-H spectrum, whereas DVB-T signals come from advertising-revenue-based local and nationwide television broadcasters.

According to Rayfield, no cellular-service provider and, therefore, no hardware partner will embed handset support for a feature unless, when a consumer uses the feature, it translates into tangible revenue for the carrier. "The last time the cellular-service providers added a low- to no-revenue feature was the camera phone." Rayfield also pointed out that cellular phones don't tune in AM- or FM-radio transmissions. "And they didn't add the camera feature out of charity; they thought it'd be highly profitable, although it didn't turn out that way," he said (**Reference 2**).

The cellular-versus-broadcast-service tug of war that Rayfield suggests is occurring in Europe is also likely to exist in any country in which revenue- and profit-fueled open-market conditions determine business success or failure—that is, when a government or another organization doesn't heavily subsidize the service. The struggle is occurring in the United States, where over-the-air-TV broadcasters have over time increasingly seen their direct-access audience shrink; consumers are instead indirectly viewing broadcasters' content using cable, IPTV (Internet Protocol television), satellite, and other service intermediaries. In such a scenario, lucrative advertising revenue flows directly to the intermediaries, not to the broadcasters, and content-licensing fees don't make up the shortfall.

Now, another set of potential delivery intermediaries, the cellular-service providers, is entering the picture. Several US broadcast-network and local-affiliate representatives paint the mobile-phone carriers as competitors, though none of them will go on record as saying so. This reluctance is no surprise, because the carriers are also these networks' and affiliates' partners, and a public statement critical of that relationship might adversely affect the licensing-fee-revenue flow. Despite that reluctance, the networks and affiliates do worry about the long-term fiscal impact of having only a supporting role in the mobile-TV market of the future. That concern explains the vigorous, ongoing industry development of the ATSC-M/H (Advanced Television Systems Committee-Mobile/Handset) specification.

AT A GLANCE

- Battery-draining concerns, along with consumers' preferences for free, albeit advertising-supported content, open the door to noncellular mobile-television options.
- Several proposals, now operating in prototype trials, aspire to augment ATSC (Advanced Television Systems Committee) with portable capabilities.
- It's unclear whether cellular carriers' and their hardware partners' future handsets will support ATSC-M/H (ATSC-Mobile/Handset).
- Satellite-delivery schemes are location-generic but have plenty of competition and, in handheld configurations, come with power-consumption shortcomings.

ATSC SHORTCOMINGS

The developers of 8-VSB (eight-level-vestigial-sideband)-based ATSC designed it with exclusively stationary reception in mind, unlike its COFDM (coded-orthogonal-frequency-division-multiplexing)-based peers. As a result, ATSC is prone to environmentally induced factors, such as multipath-signal distortion, which causes egregious mobile-TV reception. I was witness to an example of this bad reception during a Samsung-hosted bus ride in Las Vegas at last year's NAB (National Association of Broadcasters) Conference. Sin-

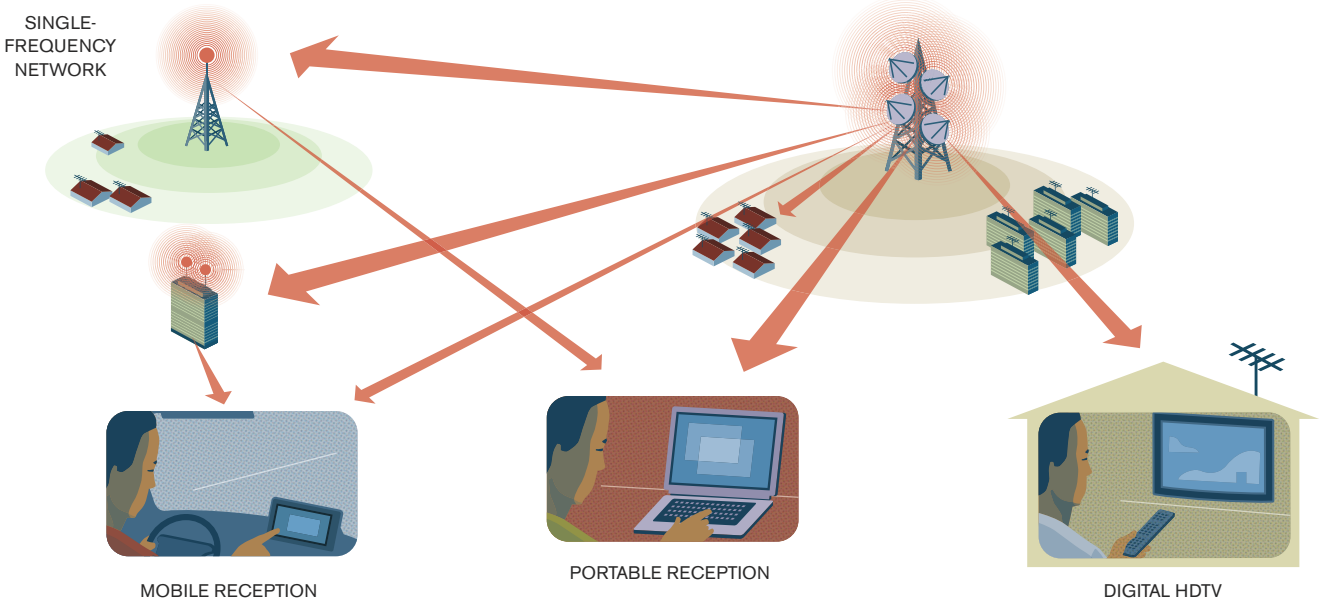


Figure 1 Samsung's A-VSB mobile-television system is amenable to both single- and multiple-antenna-network topologies.

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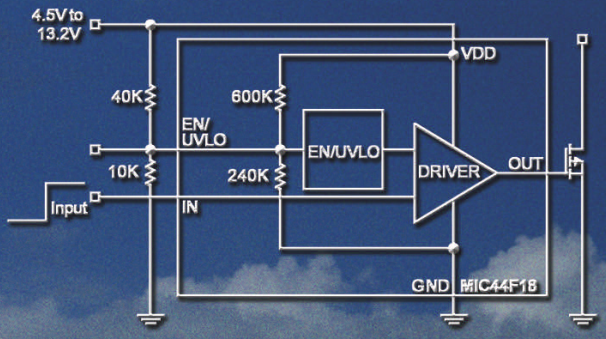

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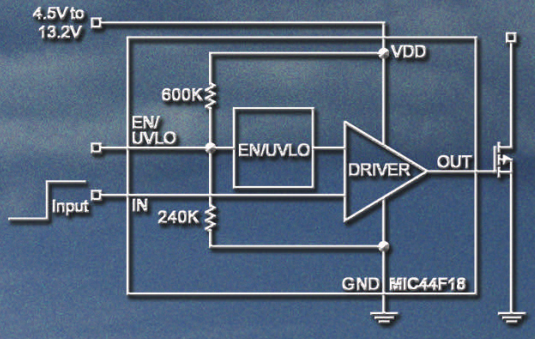

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clair-owned TV station KVMY was broadcasting ATSC-compliant images, which in-vehicle electronics received and displayed on an LCD on the rear wall of the bus. Whenever the bus was moving, artifacts corrupted the images, and, when the bus speeded up, the images disappeared altogether, despite the bus-based receiver's cognizance of the SRS (supplementary-reference-sequence) bit stream and the use of multiple diversity-reception antennas.

Two LCDs next to that one, along with Samsung-supplied UMPC (ultra-mobile-personal-computer) handheld systems, showed no artifacts, no matter how fast the bus was moving. Samsung based them on A-VSB (advanced-VSB) technology, which Samsung and Rohde & Schwarz developed. A-VSB redirects a portion of the 19.2-Mbps ATSC digital-broadcast stream away from its traditional functions—carrying Dolby Digital audio and MPEG-2 video information—instead allocating it for two mobile purposes. One purpose is a 1-Mbps SRS bit stream to assist a receiver in remaining "locked" onto the broadcast signal while in the presence of dynamic interference. The other is a variable-bit-rate turbo code for EDAC (error detection and correction) and error concealment within the audio and video streams.

Samsung privately showed A-VSB at the 2006 NAB Conference, and first public exhibitions occurred at the January 2007 CES (Consumer Electronics Show). At NAB 2007, the company simultaneously demonstrated both quarter- and half-rate turbo-coding techniques. Quarter-rate mode targets mobile-TV reception in bullet trains moving at ultrahigh speeds. The NAB demo required 1.5 Mbps of EDAC bandwidth, and Samsung bundled it with a 0.5-Mbps H.264 audio-plus-video special-content stream of 320×240-pixel QVGA (quarter-video-graphics-array) resolution. The demonstrated 19.2-Mbps "wrapper" also contained a half-rate rebroadcast of the primary ATSC content for reception in vehicles moving at highway speeds. That broadcast comprised 1-Mbps of turbo code and 1 Mbps of H.264-encoded audio/video data.

Subtracting the SRS stream and two H.264-plus-turbo-code streams, all of which a traditional ATSC receiver ignores, left approximately 15 Mbps of conventional terrestrial-digital-broadcast data. Samsung officials believe that this reduced base bit rate is still sufficient for delivering high-quality audio and video, considering the mature state of Dolby Digital and MPEG-2 encoder technology. Even more bandwidth is available for the basic ATSC stream if an application requires only one mobile-tuned turbo-code-plus-content stream.

Samsung not only demonstrated an A-VSB-enhanced signal coming from Sinclair's broadcast antenna on Mount Potosi, 25 miles southwest of Las Vegas, but also partnered with Ion Media Networks to create a SFN (signal-frequency-network) rebroadcast of Sinclair's material with low-power transmitters on the Stratosphere and Paris hotels and at the Las Vegas Convention Center acting as the source (**Figure 1**). According to Samsung's documentation, without A-VSB-enabled synchronization, echoes would overwhelm a coordination of the three transmitters' signals. Also according to Samsung's literature, SFN "enables broadcasters to cover a service area with uniform signal strength, even in hilly or built-up terrain, improving service quality."

Figure 2 Sirius's Backseat TV made its initial preinstalled appearance in a variety of Chrysler 2008-model-year vehicles and is also available aftermarket.

The April 2007 NAB also featured initial public demonstrations of MPH (mobile-pedestrian-handheld) technology, a competitive ATSC-enhancement proposal, which partners LG Electronics and Harris champion. Both A-VSB and MPH, along with a rumored third approach that Micronas and Thomson are developing, are vying for the lucrative implementation-based royalty revenues from the developing ATSC-M/H specification. MPH's developers have publicly revealed relatively little about the technology. Press coverage at the technology's March 2007 unveiling noted, "According to Harris, the proposed format provides higher signal performance as well as the ability for broadcasters to add more of a payload to the mobile part of their spectrums than A-VSB, allowing the delivery of more channels to viewers and a more robust signal. At a recent press conference in New York, the company said that low-power testing of the format demonstrated performance at approximately a 7-dB greater signal threshold than A-VSB." (**Reference 3**).

"The MPH physical layer offers a number of advantages [over A-VSB]," says Jay Andrick, vice president of broadcast technology at Harris, "including channel efficiency that scales across any number of MPH channels, full-time burst-mode transmission that translates to minimum receiver-battery drain, [and] absolute compliance and compatibility with ATSC A/110 Distributed Transmission Standard. And MPH receive devices do not rely on diversity antennas or tuner systems to achieve

MORE AHEAD

The technical capabilities and economic attributes of 4G cellular networks, such as LTE (long-term-evolution) and UMA (unlicensed-mobile-access) may make them more amenable to mobile-TV transmission than their 3G predecessors. WiMax holds similar potential, and Sprint is poised to soon launch it in the United States. For more information on all of these technologies, see *EDN's* April 3, 2008, issue, whose publication will coincide with the CTIA (Cellular Telecommunications Industry Association) Wireless show.

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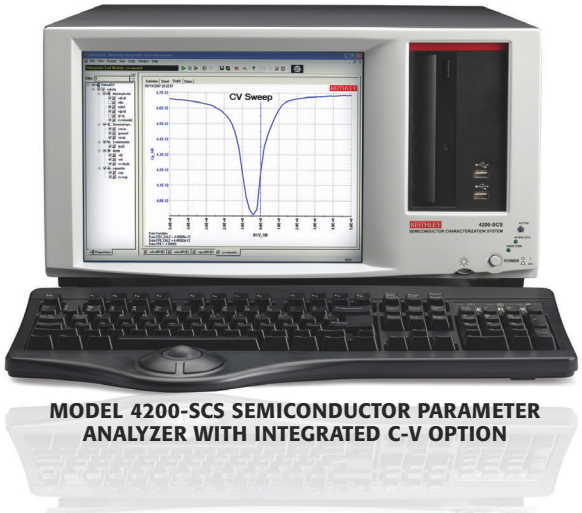

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robust reception. Recent major-market field testing has proved that MPH offers extremely reliable service to the radio horizon using a variety of handheld receiver devices."

Whether cellular carriers and their hardware-provider partners will embrace ATSC-M/H is unclear. Vendors are most likely to include the feature in "unlocked" phones and open-platform designs, such as OpenMoko's technology and Google's Android. Ever the optimists, however, the ATSC-M/H contenders claim that ATSC-enhanced broadcast TV complements rather than competes with the cellular providers' efforts in the mobile-TV arena. "A-VSB gives wireless-service providers the chance to free up crowded wireless-broadband spectrum by relying on TV spectrum as the most efficient way to deliver bandwidth-intensive broadcast video to mobile devices," according to Samsung, "while OMA-BCAST [Open Mobile Alliance Mobile Broadcast Services Enabler Suite] applications delivered along with broadcast programs will entice consumers to use those same mobile devices to access interactive services carried over wireless broadband networks."

THE ATSC-M/H CONTENDERS CLAIM THAT ATSC-ENHANCED BROADCAST TV COMPLEMENTS RATHER THAN COMPETES WITH THE CELLULAR PROVIDERS' EFFORTS IN THE MOBILE-TV ARENA.

RECOVERING THE SATELLITES

A multiantenna SFN can compensate for terrain and other inconsistencies within a given desired reception area. However, the curvature of the earth, along with other variables, such as the broadcast signal's strength and frequency, limits the coverage of any terrestrial antenna-based system. To cover a large area, such as the United States, you need a single- or multiple-satellite-broadcast scheme, such as the one Sirius Satellite Radio uses. Sirius, in partnership with Chrysler, late last year rolled out its STMicroelectronics-powered Backseat TV add-on video service. Chrysler offers the service as an option on 2008 Dodge Grand Caravans, Chargers, and Magnums; Chrysler Town & Country and 300 models; and Jeep Commander and Grand Cherokees. The factory-installed SVC1 receiver costs $470, along with a $6.99/month increment beyond the basic Sirius Radio-service price (**Figure 2**). The aftermarket manufacturer's suggested retail price is $299.99, plus installation. Chrysler-installed units come with one year of service. Back-seat passengers can watch content from the Cartoon Network, Disney Channel and Nickelodeon, and front-seat occupants can simultaneously listen to Sirius Satellite Radio.

At the 2005 CES, Microsoft and Sirius announced that Backseat TV would employ Windows Media Video as its

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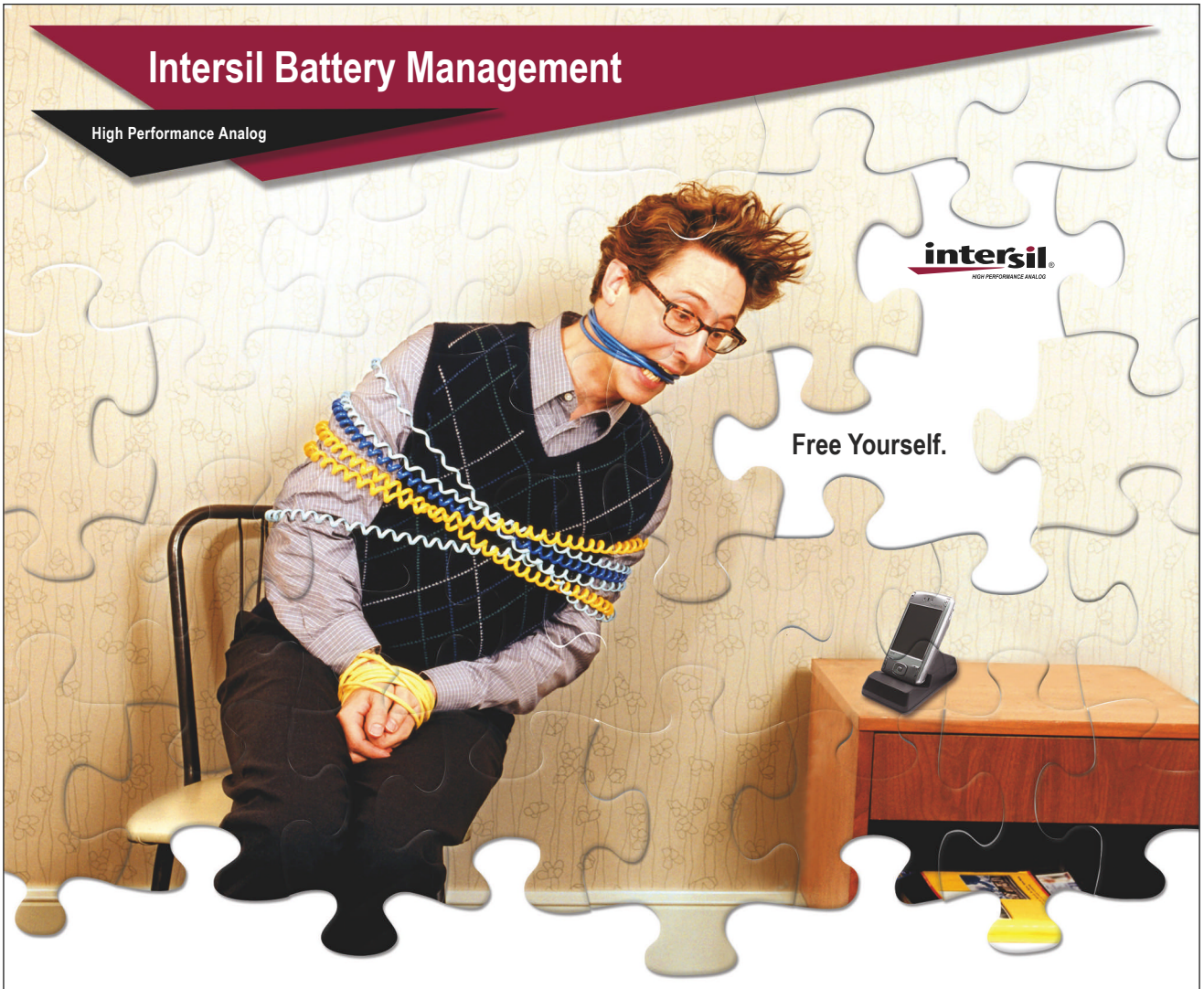

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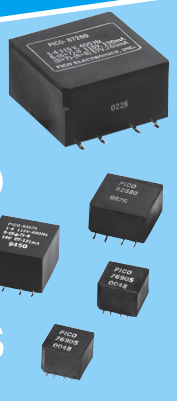
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codec technology. However, according to a recent article, Sirius ended up using a proprietary variant of H.264, also known as MPEG-4 AVC and MPEG-4 Part 10 (**Reference 4**). A demonstration of Sirius Backseat TV at January's CES left me with an impression of lukewarm video quality. The company won't reveal the material's broadcast resolution, but I estimate that I was watching, at best, low-frame-rate QVGA content on the approximately 8-in. LCD.

In comparison with a conventional single-antenna Sirius Satellite Radio setup, a Backseat TV-enhanced installation employs dual antennas—one at the front of the vehicle and one at the rear—for reception-optimizing diversity selection. Enhanced EDAC algorithms also boost reception quality. Sirius' engineers squeezed three channels' worth of audio-plus-video material into the company's 12.5-MHz S-band spectrum on top of the existing 134 channels' worth of audio-only content. Pixel artifacts aside, the fact that they were able to meet this video goal without noticeably degrading the quality of the audio content represents an impressive technical achievement.

The commercial success of Backseat TV isn't a foregone conclusion, however. Considering the diversity of alternative video-entertainment sources, such as built-in and portable DVD players, video iPods, and the like, customers might resist paying for premium equipment and service in premium-vehicle variants just to get Sirius. And what of handheld Sirius video receivers, akin to today's S50 and Stiletto series of satellite-radio-only portable units? "Sirius has never talked about portable video, as in handheld-device video," says Patrick Reilly, senior vice president of communications at Sirius. "But XM [Satellite Radio] has. There are clips on it." Note that Sirius is pursuing a merger with XM. Perhaps, as is the case with today's portable satellite-radio receivers, the option of playing back captured material that you recorded with an ac-tethered device will mitigate power-consumption concerns. So stay tuned. EDN

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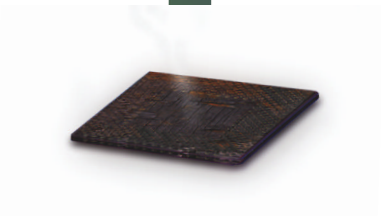
Consumer ICs: designing for reliability

CONSUMERS WANT THE LATEST ELECTRONICS BUT ONLY IF THEY'LL LAST LONGER THAN THE TIME IT TAKES TO TAKE THEM OUT OF THEIR PACKAGES. IC VENDORS MUST TACKLE RELIABILITY ISSUES SO THAT THEIR DEVICES WILL FIND USE IN RELIABLE, LONG-LASTING PRODUCTS.

BY MICHAEL SANTARINI • SENIOR EDITOR



If you've purchased a Microsoft Xbox 360 or a Sony Playstation 3, the person who sold you the system most likely recommended adding a cooling fan to go along with the game system. Chances are good that you reluctantly forked over the extra $30, even though the fan corrects what would appear to be a design flaw that shouldn't be there in the first place. And, if you were an early Xbox 360 customer, you probably received a recall notice from Microsoft offering free replacements of ICs, IC-cooling systems, or both that were prone to system slowdowns or even failures. Even if you didn't yet own a 360, you had probably heard about the recall and the likelihood that 360 may have some design flaws but then went ahead and bought one anyway.

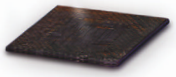
It's an increasingly interesting phenomenon in the industry: Consumers are buying products that they know are prone to early failures. In the consumer-electronics market, the drive for the latest and greatest digital "bling" often overcomes better judgment, so purchases of consumer electronics are quickly becoming emotional ones. Many people buy a new game console every four years when they become available, a new mobile phone and MP3 player every year, and a TV and PC every four to six years.

Although consumers now seem willing to fork over cash for the bling, will they be willing to do so in the future if product failures start occurring before their mobile-phone contract has expired? Even if consumers aren't worried, the makers of consumer products should be, because early defects will sooner or later cause costly recalls and may even turn consumers and OEMs against the defective brands. In the game-console world, consumers have only three choices: the Xbox 360, the PS3, and the Wii. In the TV, cell-phone, and most other consumer-electronics niches, however, consumers and OEMs have many choices—and very long memories.

Product longevity—or the lack thereof—becomes an even more daunting problem when you take into account the ever-increasing complexities of designing and manufacturing the leading-edge IC designs that power consumer devices. The semiconductor industry now focuses largely on ensuring that IC-design fabrication produces sufficient yields, that the ICs pass functional tests so they can go into products in large volumes, and that those products will land on store shelves sooner than those of the competition. But, as IC processes become more advanced and consumer demand for greater performance and system functions increase, IC failures will become more commonplace unless vendors tackle reliability issues.

Providers of military, automotive, and medical ICs have long practiced high-reliability techniques to ensure that devices last. Those designing and manufacturing ICs for the consumer and OEM market also have paid close attention to reliability, and most target an MTBF (mean time between failures) of at least 10 years—longer than most consumers will keep the products. Experts say that reliability will always be a major concern for semiconductor vendors, but these vendors must overcome many obstacles before they can produce reliable products that meet customers' increasing demands for faster, smaller, and higher performance products. Most consumer-device manufacturers employ reliability-engineering groups that set guidelines for and closely monitor designs through each step of the design, manufacturing, packaging, and burn-in processes. Burn-in is an important step because it puts designs through accelerated-lifetime tests for the best performance under worst-case conditions—high temperature and humidity. As a manufacturer develops each new silicon process, these reliability-engineering groups are constantly on the lookout for both new and re-emerging failure mechanisms (**Figure 1**). Today, they also must monitor trends, such as gate leakage and process variability, that can complicate the manufacture of reliable ICs (see **sidebar** "The shifting sands of silicon" in the Web version of this article at www.edn.com/080306cs).

"There's no such thing as the 'same old, same old' in the reliability world," says Jack Hergenrother, PhD, manager of technology for System Z Test in the IBM systems and technology group. "We've been progressing continuously in our understanding of new failure mechanisms and new ways of looking at potential wear-out and failure mechanisms." According to Hergenrother, this phenomenon is not unique to IBM. "It's an industrywide thing," he says. "In the last 10 years [as Moore's Law has evolved], some new mechanisms have come up, and you need to factor in those [mechanisms] during the qualification and design process. That [need] is true from both a chip- and a system-reliability perspective."



Experts say that the industry has been able to adequately and quickly address reliability issues at all phases of development. According to John Chen, vice president of technology and foundry operations at graphics-processor vendor Nvidia, the industry will be able to overcome these problems in the next few years. "Designers need to be aware of these issues, so they can take full advantage of advanced technology and avoid pitfalls," he says. Both Nvidia and Xilinx are in the forefront when it comes to creating designs employing new logic processes, so they and their foundry partners must be aware of potential failures, according to Glenn O'Rourke, senior director of product-development engineering in the advanced-products group at Xilinx (see **sidebar** "Fab or fabless: Reliability is still top goal"). "We more than double the [number of] transistors in our designs every 18 months because graphics engines require massive processing power," says Chen.

Nvidia's co-founder, Chris Malachowsky, in 1996 designed the company's first chip, a 1 million-transistor design that was massive for its time. In comparison, the company's latest graphics processor, which the company built using 65-nm technology, exceeds 1 billion transistors. "We can always use smaller, faster, and higher performing transistors, unlike some applications that are pad-limited and are not scalable," says Chen. "We have a great opportunity for riding the wave of Moore's Law; we are always at the forefront of the technology. However, new challenges come with being one of the first companies to use a new technology."

AT A GLANCE

- Most companies target their devices for a 10-year life expectancy and do several stress tests to ensure that their ICs will meet or exceed that goal.
- Soft errors have become bigger problems for logic-based design over the last two technology nodes.
- Companies such as Nvidia and Xilinx are typically the first to use new processes and begin working with foundry partners.
- IBM takes a holistic approach to reliability, examining potential reliability issues at the technology, device, package, and system levels.

IC-FAILURE MECHANISMS

For the 130-, 90-, 65-, and 45-nm process nodes, IC-reliability groups have paid the most attention to failure mechanisms such NBTI (negative-bias-temperature instability), hot-carrier effects, EM (electromigration), gate-oxide integrity, and SERs (soft-error rates). NBTI and hot-carrier effects are two commonly monitored failure mechanisms, both leading to a loss of gate control (**references 1** and **2**). NBTI is a key reliability issue that is of immediate concern in CMOS devices enduring stress from negative-gate voltages. Hot-carrier effects occur when an electron, or "hole," gains sufficient kinetic energy to overcome a potential barrier, becoming a "hot carrier," and then migrates to a different area of the device. In both NBTI and hot-carrier effects, the driving current to a transistor becomes smaller, degrading or locking up the timing of the gate, potentially causing failures.

The issue of NBTI became a problem at the 90-nm node, but manufacturers quickly addressed the issue. The initial studies of NBTI typically focused on devices running on always-on dc current, in which the problem is worse, according to Li-Pen Yuan, group R&D director for extraction- and power-integrity products at Synopsys. Devices running on ac have less of a problem with NBTI because the current is discontinuous, thus it does not overstress the transistors. NBTI remains an issue that reliability and design groups must monitor, however, especially if their designs target dc-system applications, such as mobile computing or handheld devices.

NBTI hasn't disappeared but has gone into the background, says IBM's Hergenrother. "A few years ago, it caused some problems," he says. "You don't hear about it too much anymore because we have figured out how to deal with it. Today, you hear more about PBTI [positive-bias-temperature instability], which is similar to NBTI, except that it happens on a PFET rather than an NFET. The physics of PBTI are different enough that it will become a problem at later technology nodes. This time, the industry will likely be more ready for it."

IC manufacturers squeeze more speed from transistors and minimize leakage power by using strain engineering—a technique for enhancing performance by modulating strain, or stress, in the transistor channel. Modulating strain enhances electron mobility and, thus, conductivity through the channel. One of the side effects of the technique is that it can introduce hot-electron effects into the design. These effects can shift the voltage threshold and reduce the lifetime of an IC. "Intuitively, if you use strain engineering, you make the transistor faster and higher power and may cause more hot-electron, or hot-carrier, effects," says Chen. He explains that strain engineering induces a higher electrical field near the drain side of the transistor and causes the electrons in

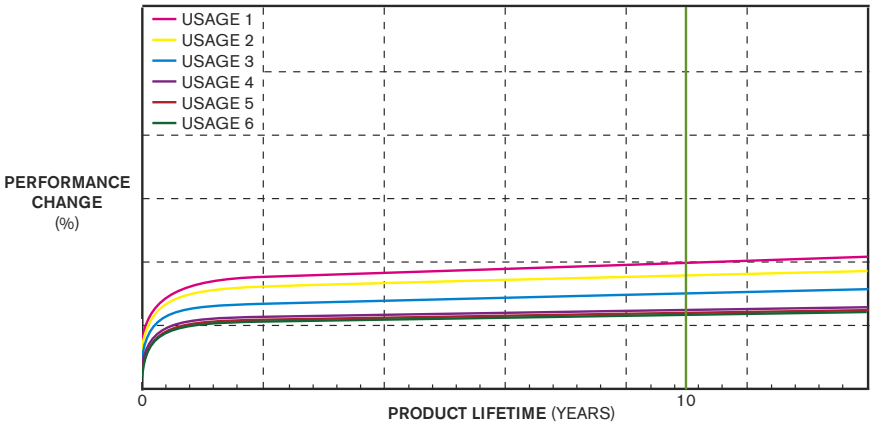


Figure 1 Xilinx devices find use in multiple applications, which in turn target long lifetimes. Xilinx uses lifetime-performance analysis, which runs full characterization during various points in the burn-in process.

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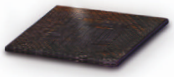


the N channel to quickly reach velocity saturation. Electrons must move as fast as they can because doing so provides current. "[The moving electron] will hit other electron-hole pairs and generate other electrons," he says. "It's an avalanche effect—impact ionization—that creates more electrons, and, when they get too much energy, they jump into the MOS-gate dielectric and get trapped there, causing a threshold shift and ultimately device failures. But manufacturers have figured out how to increase the barrier entering the gate dielectric. In that regard, it helps: It increases the hot electrons but creates a barrier to stop electrons from getting trapped in the dielectric. The net effect is equal or fewer hot-carrier effects."

The most diligently monitored failure mechanism, EM, occurs when too much current passes through thin metal traces connecting transistors. When two thin traces are close together and carrying current or switching at once, one can splinter, causing an open. This splinter can then touch the adjacent trace, causing a short circuit, which can lead to a device failure. EM usually occurs over time, leading to failures long after the chips have left testing. Both the semiconductor and the EDA industries have been aware of EM for many years. "EDA vendors offer analysis tools to detect areas of a design that are susceptible to EM," says Synopsys' Yuan. As new processes emerge, EM has grown but not excessively. "A typical design 10 years ago would have a few areas that were sensitive to EM," says Yuan. "Today, a design may have just 10 [areas]. It isn't like the problem is exploding." As EM continues to be a problem, however, tools for preventing it will likely become more common in the mainstream designer's toolbox.

Another failure mechanism is gate-oxide breakdown or integrity, in which current causes a slow breakdown of the gate dielectric, which can lead to failures. Chen notes that new materials, such as high-k-metal gates will help improve reliability in this area. Intel pioneered these materials, and the rest of the silicon manufacturers will soon follow. Chen notes that some 45-nm and, more likely, 32-nm designs will likely use high-k metal dielectrics composed of hafnium oxide instead of the more traditional gate oxide. Manufacturers grow gate oxide on the silicon during the manufacturing process, and doing so creates a remarkably smooth surface. But in high-k fabrication, manufacturers deposit the hafnium oxide on the silicon in composite layers. "If you use one type of layer, it usually doesn't work," says Chen. Using multilayer, high-k dielectric usually means hav-

FAB OR FABLESS: RELIABILITY IS STILL TOP GOAL

IC reliability is a top concern for both companies that own their own fabs and those that don't. For example, IBM creates its products in house, allowing the company to address reliability concerns and even design trade-offs at all levels of product development: technology and transistor development, circuit-level design, chip design, package design, and system implementation. "Fabless" companies, such as Nvidia and Xilinx, on the other hand, must rely on external foundries to manufacture products. And because the two companies are in highly competitive markets, they tend to be the first to jump to a new foundry's process when it becomes available. But before they begin designing with that process, they make sure it passes rigorous qualifications, such as ISO (International Organization for Standardization) 9000x, ISO 14000, and OCEA (Office of the China Economic Area) standards.

Glenn O'Rourke, senior director of product-development engineering in the advanced-products group at Xilinx, says that the company uses both UMC (United Microelectronics Corp) and Toshiba as suppliers, so Xilinx must ensure that both sources can make comparable versions of Xilinx's devices. To achieve this goal, Xilinx develops a reference model of its designs and ensures that both suppliers can meet their objectives. "We develop a silicon reference model upfront, and … both fabs drive to those goals," says O'Rourke. He also notes that, because Xilinx's chips find use in a variety of applications, the company analyzes its designs' lifetime performances (Figure A). "We do an accelerated burn-in to mimic the lifetime of the product," he says. "We do full characterization across temperature and voltage to see how the product's performance is changing over its lifetime. We leverage that data to cover the usage and the specifications for the lifetime of the product." Xilinx then makes the results of those reports available to customers.

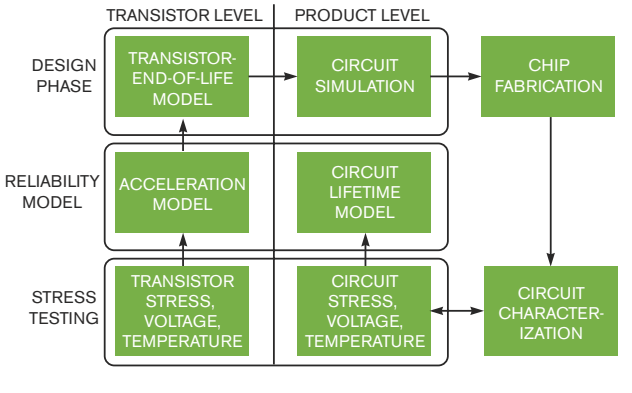
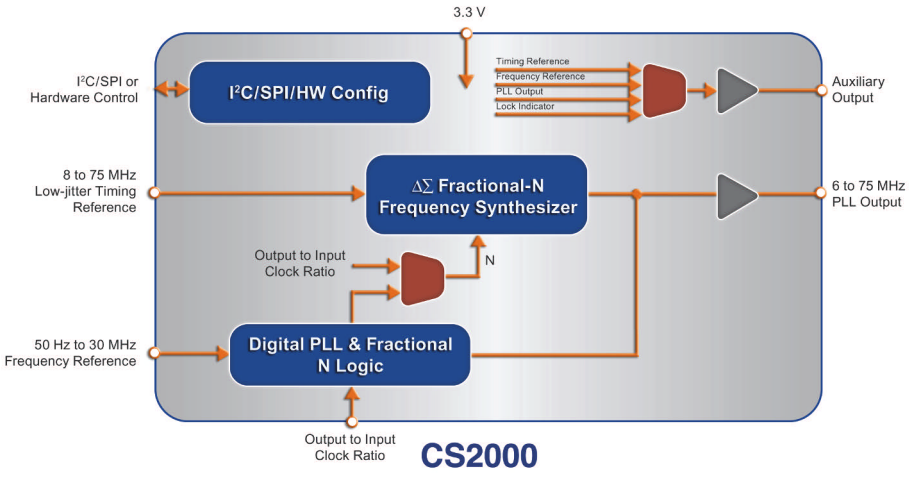


Figure A Xilinx and other large companies examine reliability at multiple phases in IC development.

Cirrus Logic's Clocking ICs Offer Superior Low-Noise Performance

Clock Generator and Low-Jitter Clock Multiplier in a Single IC



Host Interface	One-Time Programmable	Frequency Synth/Clock Generator	Clock Multiplier/Jitter Remover	Power Supply (V)	Input Frequency Range	Reference Frequency Range	Output Frequency Range	Package
CS2000-CP	CS2000-OTP	✔	✔	3.3	50 Hz to 30 MHz	8 to 75 MHz	6 to 75 MHz	10 MSOP
CS2100-CP	CS2100-OTP	—	✔	3.3	50 Hz to 30 MHz	8 to 75 MHz	6 to 75 MHz	10 MSOP
CS2200-CP	CS2200-OTP	✔	—	3.3	—	8 to 75 MHz	6 to 75 MHz	10 MSOP
CS2300-CP	CS2300-OTP	—	✔	3.3	50 Hz to 30 MHz	Internally Generated	6 to 75 MHz	10 MSOP

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- Clock generation/frequency synthesis
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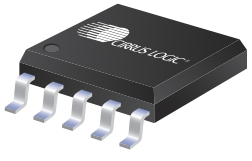

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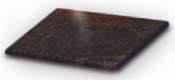

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ing fewer pin holes because it's harder to align pin holes for multiple layers. Using high-k dielectric materials usually improves time-dependent-dielectric-breakdown performance. However, unlike silicon dioxide, composite layers have more traps, and more traps can cause electron or N- or P-channel hole trapping, which can cause soft breakdowns, he says. Those things degrade mobility and, in the long term, can create threshold instability. The manufacturers have come up with various process tricks to overcome this issue. "One way is to put a silicon-dioxide layer between the high-k-metal layer and the silicon," says Chen.

SER, another failure mechanism that has long been a concern in the military- and aerospace-IC and memory markets, is now becoming a greater concern in logic devices (**Reference 3**). Alpha particles in packaging materials or neutron strikes that occur naturally in the environment are the typical causes of soft errors. Essentially, an alpha particle or neutron can strike a device, generate noise, and flip bits in memory devices or even flip latches in your circuit. "It is getting to be a bigger challenge with each technology generation," says IBM's Hergenrother. "At the active areas of the devices, the volume of the critical-area devices keep going down, which means that you have to deposit smaller and smaller amounts of charge to create an upset in your transistor." It's difficult to remove alpha particles from packaging materials, so you must build immunity to both cosmic and alpha particles into your system. You can address soft errors at many levels. "[IBM] looks at SER at the technology level to make transistors soft-error-tolerant, at the circuit level … to arrange transistors into latches and flip-flops so that it is robust even if one of the transistors does flip," he says. "Then, we look at the chip level for robust error-detection and -correction mechanisms, so, even if there is an error, we catch it and correct it before it propagates any undesirable data. On top of those mechanisms, we have system-level protection, which is another layer of error detection and correction."

Several failure mechanisms can lead to reliability issues. The semiconductor industry has been diligent about identifying and thus correcting failure mechanisms before they ever reach consumers. As devices move closer to the limits of physics and CMOS, however, you may wonder whether reliability will become a worse problem to deal with. EDN

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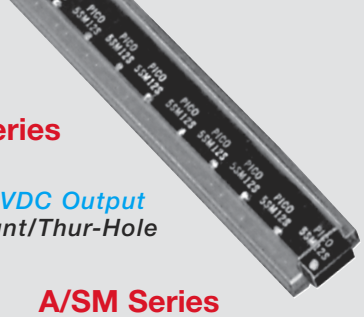

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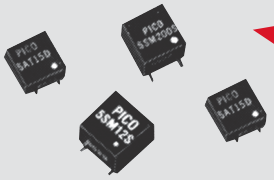

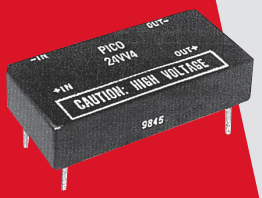

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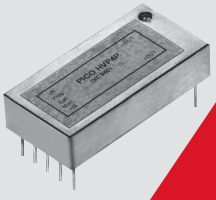

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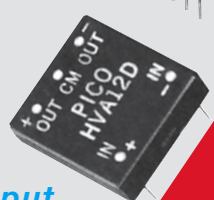

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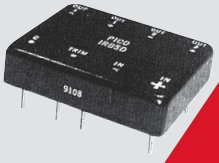

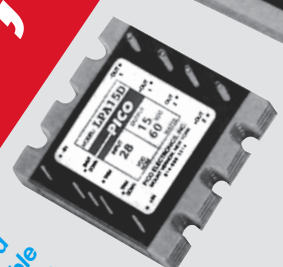

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Designing with QDRII+ and QDRII in one system

ALTHOUGH THE LATEST QDRII+-SRAM DEVICES OFFER SPEEDS AS MUCH AS 50% HIGHER THAN QDRII PRODUCTS, A PROPERLY DESIGNED BOARD CAN SUPPORT EITHER ARCHITECTURE.

Memory devices are evolving to match the needs of applications that are in continuous demand, such as high-performance communications, networking, and DSP systems. Specialized memory products that optimize some architectures' memory bandwidth have successfully increased the overall performance in a variety of data-processing systems, and operating speeds have increased to as much as 500 MHz. To meet the demand for these products, the QDR (quad-data-rate) Consortium, which comprises Cypress, IDT, NEC Electronics, Renesas, and Samsung (www.cypress.com, www.idt.com, www.nec.com, www.renesas.com, www.samsung.com), has released the next generation of SRAMs. The QDRII+ (quad-data-rate II+) SRAMs meet these requirements by offering higher memory bandwidth, improved timing margins, and more flexibility in system designs. QDRII+ SRAMs offer 50% higher speeds than QDRII SRAMs, deliver a bandwidth as high as 72 Gbps, and come in FBGA packages. The QDRII+ architecture uses the currently installed infrastructure to create higher performing products and allows a direct transition to higher frequencies.

QDRII and QDRII+ devices have two independently operating ports that run at twice the selected clock rate, allowing a transfer of four data words across the two ports in a single clock cycle. QDRII and QDRII+-SRAM devices provide concurrent reads and writes, allowing simultaneous access to the same address location. This innovative architecture provides four-times-better performance than other SRAM devices in networking applications. These devices suit bandwidth-intensive, low-latency applications, such as controller-buffer memory, statistics memory, look-up tables, and linked lists.

QDRII AND QDRII+-SRAM OVERVIEW

QDRII and QDRII+ SRAM can perform two data writes and two data reads per clock cycle. They use one port, D, for writing data and another port, Q, for reading data (see **sidebar** "QDRII- and QDRII+-interface signals"). These unidirectional data ports support simultaneous reads and writes and allow back-to-back transactions without the contention issues that can occur when using a bidirectional data bus. Write and read operations share the address ports. QDRII and QDRII+-SRAM devices use input clocks K and K# to control the input signals, output clocks C and C# to control the output data bus only in QDRII SRAMs, and source-synchronous echo clocks CQ and CQ#.

The architecture supports burst-oriented write and read operations, and all the data-bus-width configurations support burst lengths of two and four. Both burst-of-two and burst-of-four QDRII- and QDRII+-SRAM devices provide the same overall bandwidth at a given clock speed. QDRII-SRAM devices use either the 1.5 or the 1.8V HSTL (high-speed-transistor-logic) Class I I/O standard, whereas QDRII+-SRAM devices use only the 1.5V HSTL Class I I/O standard. QDRII- and QDRII+-SRAM devices use an internal DLL (delay-locked loop) to align the data's edge with the input clocks. You can optionally turn off the DLL, but doing so degrades the performance of the QDRII and QDRII+-SRAM devices. All timing analyses in this article assume that the DLL is on. QDRII- and QDRII+-SRAM devices also offer programmable-impedance output buffers. You program the output buffers by terminating the ZQ pin to V_{SS} through resistor RQ. The value of RQ should be five times the desired output impedance—175 to 350Ω—with a tolerance of 15%.

QDRII+-SRAM FEATURES

QDRII+-SRAM architectures typically find use in high-performance networking and communication applications supporting frequencies as high as 500 MHz. The designers of this new communications-memory standard developed it for network switches, routers, and other communications applications. The QDRII+-SRAM devices extend the QDRII family of SRAMs in frequency and performance. The QDRII+ SRAM devices function similarly to a QDRII SRAM but have slight differences in the timing. However, because they have similar performance, you can use them interchangeably with only a few changes to the memory controller and the board, depending on the application. Designing the system to accommodate both QDRII and QDRII+ paves the way for higher performance in the QDRII designs.

DESIGN CHANGES FOR QDRII AND QDRII+

QDRII and the QDRII+ SRAMs differ in ac and dc parameters due to the higher speeds of operation in QDRII+. The major differences are that QDRII+ has a higher read latency, has no C or C# clocks, employs a QVLD (output-valid-indicator) pin, uses slightly different pinouts, and has different timing parameters. Higher read latency enables higher frequency operations. Hence, the design should support speeds to 500 MHz, and you should terminate the data signals. The QDRII has a read latency of 1.5 clock cycles, whereas the QDRII+ supports both 2- and 2.5-clock-cycle read latencies. The memory controller should support either 2 or 2.5 cycles of latency, and you should make this choice early in the design definition, based on the bandwidth and host-controller capabilities. At speeds greater than 250 MHz, the CQ and CQ# echo clocks clock

the data from the SRAMs; hence, QDRII+ requires no C and C# clocks, and the memory controller should use echo clocks CQ and CQ# to latch the read data from the SRAM when using QDRII+. For easier board design, QDRII+ adds a QVLD pin, which aligns with the edge of the echo clocks and occurs a half-cycle before the valid data. Hence, you should modify the board to include the QVLD signal and to take advantage of it when designing for QDRII+. QDRII devices use the P6 and R6 balls as a NC (no-connect) ball, requiring that designs using QDRII+ devices not to use output clocks C and C#. Also, Ball P6 should be pulled high with a 1-kΩ resistor. This approach helps in disconnecting the resistor to float the ball when designing with QDRII+. In DDRII+ (double-data-rate II), because it does not support linear-burst addressing, balls A0 and A1 are nonconnects. QDRII+ has a 2048-cycle DLL-lock, whereas QDRII has a 1024-cycle time. QDRII+ also modifies the tKHK#H (K-clock-rising-edge-to-K#-clock-rising-edge) parameter to 42.5% from 45% of the input-clock cycle.

QDRII+ devices let designers achieve high performance and bandwidth for their designs with few changes to boards and to create new designs. By designing boards and host controllers to meet both QDRII and QDRII+ requirements, systems can support speeds as high as 500 MHz or bandwidth as high as 72 Gbps without changing boards or host controllers. EDN

AUTHOR'S BIOGRAPHY

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QDRII- AND QDRII+-INTERFACE SIGNALS

Table A lists the clock, control, address, and data signals for pins on QDRII (quad-data-rate II)- and QDRII+-SRAM devices. A detailed description of these interface signals follows.

QDRII and QDRII+-SRAM devices have K and K# input clocks, C and C# output clocks (QDRII only), and CQ and CQ# echo clocks. The positive input clock, K, is the logical complement of the negative input clock, K#. Similarly, C and CQ are complements of C# and CQ#, respectively. The QDRII- and QDRII+-SRAM devices use the K and K# clocks for write accesses and the C and C# clocks for read accesses. CQ and CQ# are the source-synchronous output clocks from the QDRII- or the QDRII+-SRAM device that accompanies the read data. The number of loads that the K and K# clocks drive affects the switching times of these outputs. When a controller drives a single QDRII- or QDRII+-SRAM device, C and C# are unnecessary because the propagation delays from the controller to the QDRII- or QDRII+ SRAM device and back are the same. To reduce the number of loads on the clock traces, QDRII- and QDRII+-SRAM devices also have a single-clock mode, which uses the K and K# clocks for both reads and writes. QDRII- and QDRII+-SRAM devices still use CQ and CQ# for the echo clock from the memory device to the memory controller. In this mode, the C and C# clocks tie to the supply voltage.

The memory-controller device provides the K and K# clocks and the data, address, and command lines to the QDRII- or QDRII+-SRAM device. For the controller to operate properly, the write data (D), address (A), and control-signal-trace lengths and propagation times should be equal to the K and K# clock-trace lengths. QDRII and QDRII+ SRAMs generate echo clocks CQ and CQ#, which are edge-aligned with the read data. The memory-controller device usually phase-shifts the CQ and CQ# signals and uses them to capture the read data. The CQ and CQ# signal-board trace length between the QDRII or QDRII+ SRAM and the controller should be equal to the read-data (Q) board-trace length to minimize the skew between these signals.

QDRII and QDRII+ SRAM devices use two unidirectional data buses, D and Q, for writes and reads, respectively. QDRII+ SRAMs also have a QVLD (output-valid-indicator) pin. The QVLD signal aligns with the echo-clock edge and is high for approximately half a clock cycle before data is output from the memory. QDRII and QDRII+ SRAMs use the WPSn (write-port-select) signal to control write operations and the RPSn (read-port-select) signal to control read operations. The BWSn (byte-write-select) signal tells the QDRII or QDRII+ SRAM which byte to write into the QDRII or QDRII+ SRAM device. QDRII and QDRII+ SRAMs use one address bus (A) for both read and write addresses.

TABLE A CLOCK, CONTROL, ADDRESS, AND DATA SIGNALS FOR PINS ON QDRII- AND QDRII+-SRAM DEVICES

Pin	Description
D	Write data
Q	Read data
K	Write clock
K#	Inverted write clock
C[1]	Read clock
C#[1]	Inverted read clock
CQ	Echo clock
CQ#	Inverted echo clock
WPSn	Write-port select
RPSn	Read-port select
A	Address
BWSn	Byte-write select
QVLD[2]	Output-data-valid indicator

[1] QDRII+ SRAMs do not offer C and C# clocks. When interfacing with one QDRII- or QDRII+-SRAM device, the memory-controller devices use the single-clock mode, in which the QDRII- or QDRII+-SRAM device's C or C# port ties to the supply voltage.

[2] Only QDRII+ devices offer the QVLD signal.

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Several switching-converter topologies exist for power converters that operate from the ac mains and must maintain a power factor of 0.9 or better. One topology is a boost converter with a control circuit that measures the switch current and adjusts the switching duty cycle so that the input current tracks the rectified input-ac voltage. However, the output voltage is high—approximately 200V dc in the United States and more than 400V dc in Europe—and has no fixed ground reference. Because of these drawbacks, a second converter, typically a flyback transformer, provides isolation from this high dc voltage, allows a safety ground reference, and provides a regulated lower output voltage of 5 to 25V dc. The addition of this second stage adds extra components and inefficiency: Even if each conversion is 90% efficient, the overall efficiency is only 81%.

In addition, a ripple voltage always exists for a constant load on the dc output. As the single-phase ac input voltage twice passes through zero during each cycle, the load can't draw power because both the input voltage and the input current are near zero. Thus, during these voltage-crossover times, the output capacitor must supply the total load current. You can arbitrarily reduce the ripple voltage on the dc output of the boost converter by increasing the output capacitance but at a cost: In the usual case, another step-down switching converter follows the dc output of the boost converter, so a moderate amount of input ripple is acceptable because the second converter easily regulates it out.

A single-stage-transformer-flyback topology operates from ac-line voltage but has a different switching control that directly gives an isolated low-voltage output at a high power-factor figure (**Figure 1**). Because the design must handle high dc voltages only once and provides low output voltages, the topology uses an isolation flyback transformer. Because the current from ac mains to a flyback transformer is discontinuous, however, the circuit requires a different switching-control scheme to ensure a good power-factor figure. You accomplish this control by appropriately varying the duty factor of the switching converter. For practical reasons, the duty factor should be at least 35 to 40% to keep the voltage and current stresses on the switch at reasonable levels. The new control scheme also assumes a nearly constant error voltage V_E, a scaled and integrated difference between the desired output voltage and a reference voltage, throughout one half-cycle of the ac input. The control scheme also requires continuous current in the flyback transformer.

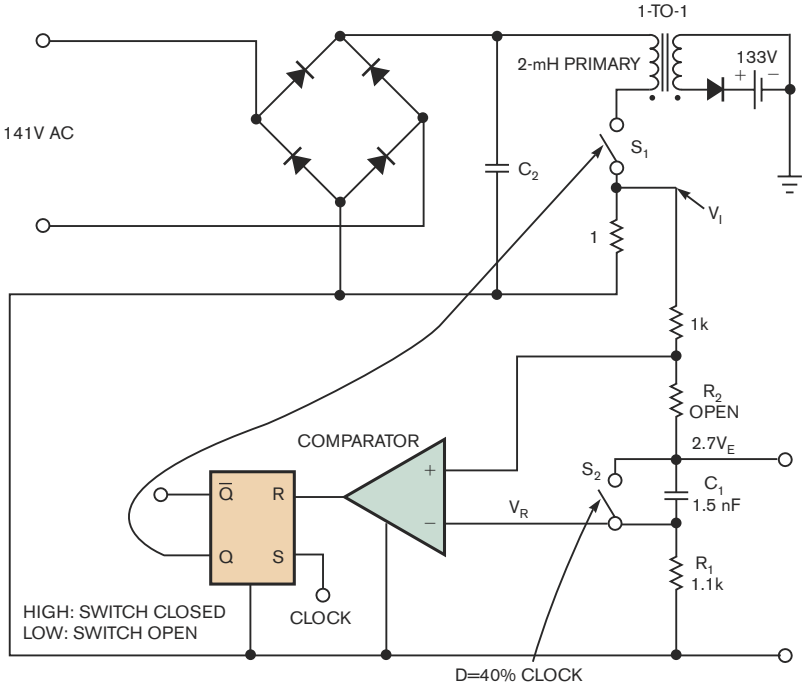

Figure 1 This single-stage transformer-flyback topology for an external power supply operates from ac line voltage but has a different switching control that directly gives an isolated low-voltage output at a power factor of 0.9 or more.

At the beginning of each switch cycle, the control circuit turns on switch S_1. The switch's current through the 1Ω resistor produces the input voltage, V_I, and a nonlinear voltage ramp, V_R, is generated. As the switch current increases while the switch is closed, V_I increases, and, when V_I intersects this nonlinear ramp, the switch turns off and remains off for the rest of that switching cycle. At the beginning of the next cycle, the switch turns on, the nonlinear voltage ramp resets, and the process repeats.

AN EXAMPLE

The converter in **Figure 1** has a maximum 141V-ac sinewave input, corresponding to a peak voltage of 200V, and runs at a 100-kHz switching frequency. The flyback transformer has a primary inductance of 2 mH; the minimum duty factor, D, is 0.4; and the error voltage is 2.7V. Although the transformer's secondary can have any turns ratio that produces the required output voltage, for this example, assume a 1-to-1 turns ratio and a secondary voltage of 133V. This secondary voltage ensures a duty cycle of 0.4 when the input sinewave is 200V. Throughout the rest of the sinewave's voltage input, the duty cycle is greater than 0.4. This set of parameters presents a 100W load to the ac input: 141V rms×0.7A rms.

For this example, **Figure 2** shows the plot of the special nonlinear curve, or ramp, along with several voltage and current operating points. The nonlinear ramp remains at 2.7V until the duty factor reaches 0.4, at which point the ramp

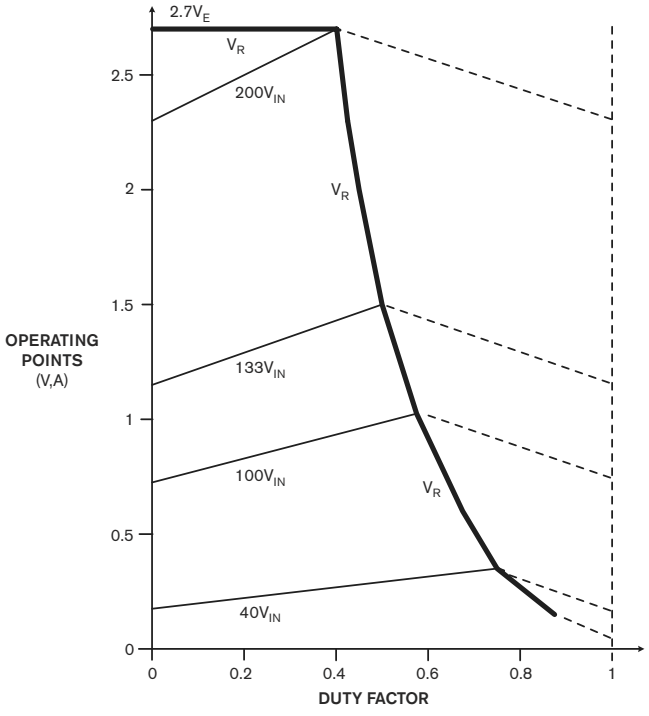

Figure 2 The nonlinear ramp voltage remains at 2.7V until the duty factor reaches 0.4, at which point the ramp voltage begins to fall.

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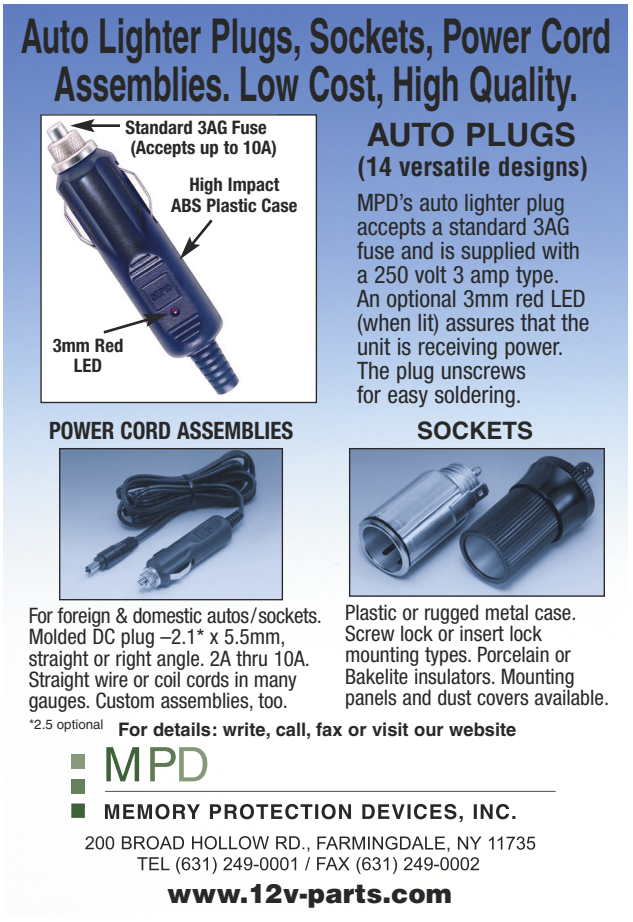
begins to fall with a substantial curvature, which is an advantage. To understand the converter's operation in this example, first consider the switching operation when the peak input ac voltage is 200V and the average input current is 1A. At the beginning of a cycle, switch S_1 turns on, and, at this instant, the switch carries 2.3A, so V_1 is 2.3V. As time passes, the inductor current and the voltage ramp up. When 40% of the cycle completes, the voltage rises to 2.7V, which intersects V_R (boldfaced line in **Figure 2**). At this point, the comparator turns off switch S_1, which remains off for the remainder of this cycle. From this 40% point until the 100% point, the flyback transformer dumps its current into the 133V load (the dashed line in **Figure 2**). At the end of the cycle, the flyback current returns to its original starting point of 2.3A. This cycle repeats when the input ac is 200V.

As the input ac voltage drops from its peak of 200V to, say, 133V, the voltage ramp changes sharply. With 133V input and 133V output, the new duty factor is 50%. Additionally, the average input current, I_{IN}, at 133V is 133/200, or 0.665A. At an input voltage of 133V, the switch current begins at approximately 1.16A and ramps up to approximately 1.5A at the point on **Figure 2** where it intersects the voltage ramp at a 50% duty factor. S_1 turns off, and the flyback transformer dumps its current into the load. The secondary current decays (dashed line) and ends at 1.16A. Note that all the secondary-current decays for all input voltages have the same slope because the transformer always discharges into a constant 133V. Thus, for all parts of the input ac voltage, this control method gives proper control of the average input current such that the overall power factor is near 100%. And, if the output load is, for example, 50W rather than 100W, the feedback-error voltage is 1.35V. The ramp voltage remains the same shape but becomes half-amplitude, so the input currents at all input voltages are half, and the power factor remains near 100%.

TO CALCULATE THE SHAPE OF THE RAMP VOLTAGE, DETERMINE THE MAXIMUM OPERATING AC VOLTAGE AND HENCE ITS PEAK.

To calculate the shape of the ramp voltage, determine the maximum operating ac voltage and hence its peak—for example, 141V rms and 200V, respectively. Then, select the switching frequency of the converter—say, 100 kHz or a period of 10 µsec. Taking into account maximum switch voltage and current stresses, select the minimum duty factor—for example, 40%, which corresponds to 4 µsec. Determine the maximum peak power this flyback converter must handle, such as 200W, corresponding to peaks of 200V and 1A. Then, determine the value of the primary inductance to give acceptable switching-current ripple—say, 2 mH. Assume continuous current in the



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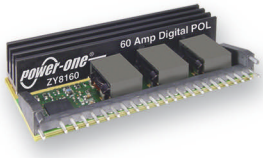

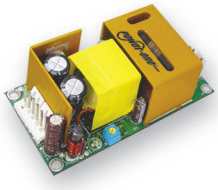

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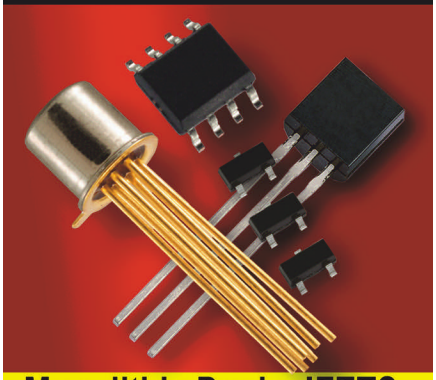
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transformer. Knowing the transformer secondary voltage and the turns ratio, calculate the flyback voltage across the transformer primary when switch S_2 is off—say, 133V.

At a maximum input voltage of 200V, average input current should be 1A. For a peak voltage of 200V and a duty factor of 0.4, the current ripple, ΔI, is $(V \times \Delta t)/L = (200 \times 4\ \mu sec)/2\ mH = 0.4A$ p-p or 0.2A pk. Because the switch is on for a duty factor of 0.4, the average current during the switch's on time is 1A/0.4, or 2.5A. Knowing that the peak current ripple is 0.2A, the current at the end of the on time is 2.5+0.2, or 2.7A. (Current at the beginning of the on time is 2.5−0.2, or 2.3A.) You now know one point on the voltage ramp: For a duty factor of 0.4, the switching current is 2.7A. With this maximum peak current, the corresponding error voltage is 2.7V.

Likewise, calculate the points for all voltages lower than 200V. For example, when the input voltage during part of the sinewave input is 100V and when the error voltage remains at 2.7V, the average input current is 0.5A. With an input voltage of 100V, the new duty factor is $133/(V_{IN}+133)$, or 0.57; the average current during the on time is 0.5A/0.57, or 0.876A; and the peak ripple current is 0.143A, so the current at turn-off is 0.876+0.143, or 1.02A. Thus, this new 100V point on the ramp voltage is a duty factor of 0.57 and a current of 1.02A.

This ramp shape applies only to a ramp voltage of 2.7V for this example. That is, the scaled shape of this ramp curve differs slightly as the error voltage changes. If you plot the ramp curve for $V_E=1V$, corresponding to a load of approximately 37W, the resulting curve differs slightly from the curve for an error voltage of 2.7V scaled by the factor of 1/2.7, or 0.37. The inductor current has ripple. Without ripple, curve scaling would be exact. For most practical applications, this slight variation is of no consequence because the resulting power factor is still excellent.

The shape of this ramp looks suspiciously like a decaying exponential of a discharging RC circuit, and, if you use appropriate values, you can almost exactly match the shape. For this example, appropriate values are 1.1 kΩ for R_1, 1.5 nF for C_1, and 2.7V for the discharging voltage. Thus, this new control circuit needs no special circuits or operational amplifiers to generate a voltage-comparison ramp; it requires just a simple RC circuit with a switch to discharge the capacitor to 0V at the end of each cycle and hold the voltage at 0V until the duty factor reaches 0.4, at which time the switch opens, and the exponential discharging curve begins. Discharging continues until the curve approaches 0V when the duty factor is 1. By varying the value of R_1, R_2, and C_1 in **Figure 1**, you can make approximations to the "ideal" ramp-voltage curve. For this example, R_2 is open, and the fit to the ideal ramp-voltage curve is excellent. Even crude approximations to this ideal curve still yield power factors of 95% or more, so wide component tolerances are acceptable.

WALL WART VERSUS FLYBACK

Millions of battery-powered consumer products need an external power supply to recharge the batteries or operate from line voltage. These chargers are typically simple "wall warts" that you plug into ac sockets. Each wall wart comprises a basic step-down transformer, a full-wave-bridge rectifier, and an output-filter capacitor. These simple, rugged, inexpensive, and reliable devices provide excellent high-voltage isolation. Their main drawbacks are poor efficiency; large bulk and weight; wide dc-output voltages due to line and load changes; and low power factors—that is, they draw huge current peaks at just the peak of the ac voltage. A typical 15V-dc, 25W wall wart might have a power factor of only 70%. Even with a large-value output-filter capacitor, ripple might typically be approximately 300 mV p-p. If the load varies by a ratio of 3-to-1 and the line varies by ±20%, the dc output voltage can easily vary from 11 to nearly 20V. Despite this wide dc-output range, wall warts are adequate for many consumer devices because the power supplies inside these devices easily regulate out the ripple and the wide output-voltage range. At light loads and high ac-mains voltage, a wall wart may provide efficiency approaching 90% but a power factor of only 60%. At heavy loads and low ac-line voltage, efficiency may be less than 75%, and the power factor may be approximately 75%.

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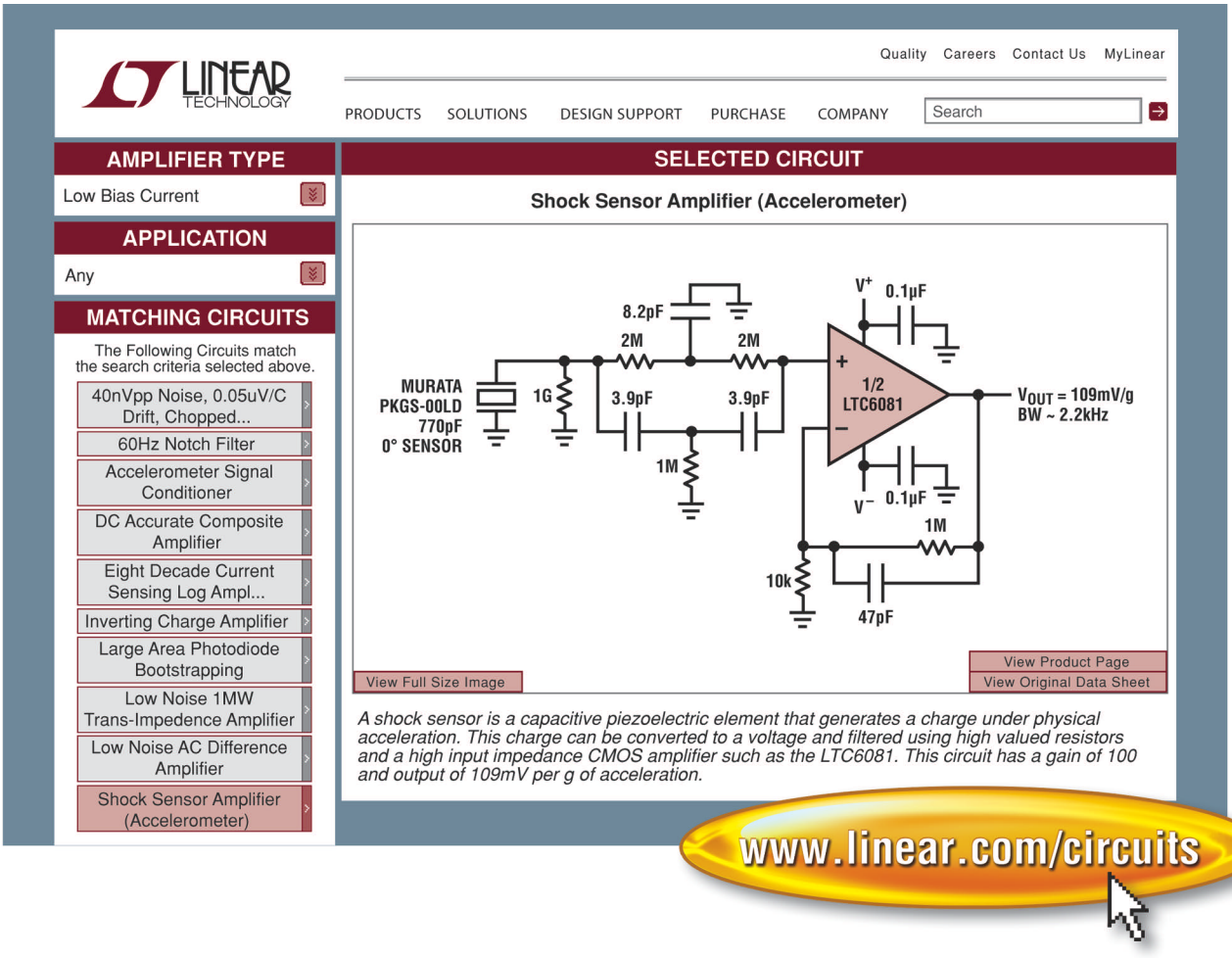

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LTC6087	1	750	14	1.2	2	General Purpose	MS-8, DFN-10
LTC6088	1	750	14	1.2	4	General Purpose	DFN-16, SSOP-16
LTC6078	0.2	25	0.75	0.072	2	TCV_{OS} = 0.7µV/°C Max.	MS-8, DFN-10
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LTC6244	1	100	50	5.8	2	Low Frequency Noise = 1.5µV_{P-P}	DFN-8, MS-8

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OVERVOLTAGE PERFORMANCE

This example assumes a minimum duty factor of 40%, which corresponds to a maximum input-voltage peak of 200V. What happens if the ac line input has a momentary overvoltage of, say, 300V and an error voltage of only 2.7V? Using the ramp of **Figure 2** and knowing that the flyback voltage is 133V, the duty factor must be 0.307 and must lie on the ramp-voltage curve. But this point lies on the X axis because the ramp voltage doesn't start to decrease until the duty factor reaches 40%. Thus, the peak current when the input voltage is 300V is just 2.7A. From this peak current point and knowing that the inductance is 2 mH, you can easily calculate the average current during the switch's on time, 2.47A, and the average input current, just 0.76A over the switching cycle. That is, the average input current, 0.76A, when the input voltage is 300V is less than the average input current, 1A, when the input voltage is 200V. Thus, this control circuit has an advantageous current-limiting property during input-overvoltage surges.

ADDITIONAL COMPONENTS

This new converter-control circuit doesn't show many of the other components you would need to build a complete switching converter. Capacitor C_2, which handles only the high-frequency switching currents, looks almost like an open-circuit at the low ac-mains frequency. The flyback transformer needs a snubber circuit. Because much of the operation happens for duty factors greater than 50%, the circuit also requires slope compensation to ensure stability. If the switch current hasn't ramped up to the V_R voltage before the duty factor reaches 100%, the control needs a default, such as 95% duty factor, to turn off the switch for that cycle. The circuit also most likely requires a limiting method for controlling the maximum value of the error voltage. The circuit will also need components to control conducted emissions if the value of C_2 is too low.

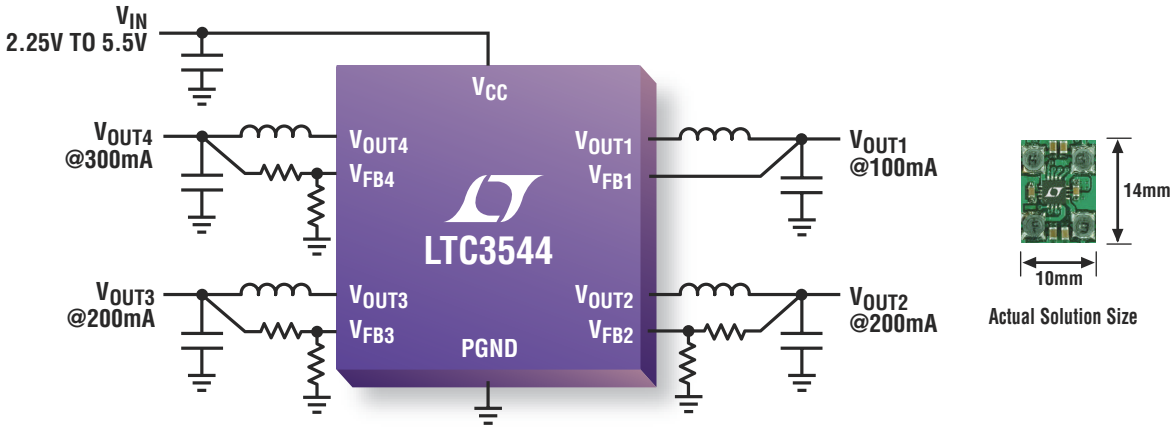
The single-stage power-factor flyback converter probably won't meet the needs of applications requiring low output-voltage ripple and fast transient response because the feedback loop of the power-factor flyback converter is deliberately slow. Also, the circuit has no location for drawing power when the ac input twice goes through zero during cycle. So, the output capacitor must supply all the output-load current. Therefore, the output must have 120-Hz ripple for a 60-Hz line voltage; the amount of ripple depends only on the size of the capacitor. You could use a traditional boost-PFC (power-factor-correction) converter and follow that part with a separate step-down converter. This approach uses more parts but provides isolation, fast transient response, and low ripple.

Because the load of this power-factor-correction flyback converter must tolerate some amount of ripple, the load may also be able to tolerate a looser voltage regulation. In this case, the power-factor-correction flyback converter can probably use the primary flyback voltage for adequate output-voltage regulation. This approach would save the cost of implementing an optical coupler and its associated circuit. EDN

AUTHOR'S BIOGRAPHY

Cecil Deisch is a staff engineer at Tellabs Operations Inc, where he has worked for 15 years. He has a master's degree in electrical engineering from New York University (New York) and holds Patent No. 4,148,097 for peak current control for PWM (pulse-width-modulated) switching converters. His other interests include thermodynamics, economics, and mathematics.

Quad Buck



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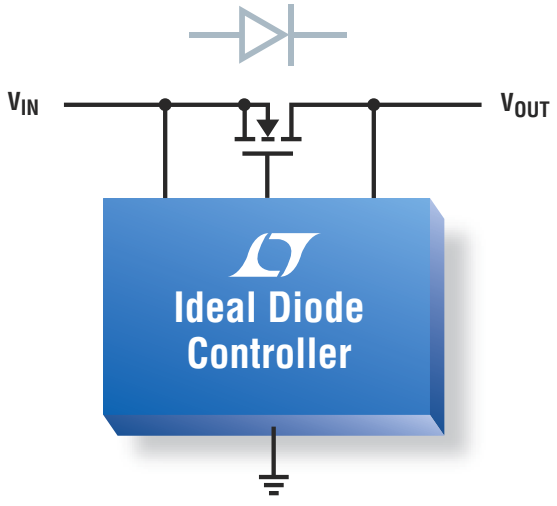

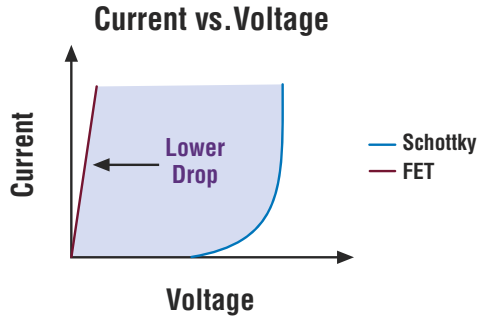

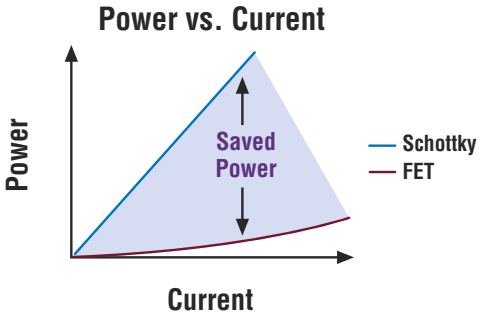

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LTC4355	9V to 80V	Dual	Yes	3 x 4 DFN-14, SO-16	
LTC4357	9V to 80V	Single	No	2 x 3 DFN-6, MSOP-8	
LT®4351	1.2V to 18V	Single	Yes	MSOP-10	

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LINEAR TECHNOLOGY

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designideas
READERS SOLVE DESIGN PROBLEMS

Audio equalizer features transimpedance Q-enhancement topology

Herminio Martínez, Encarna García, and Eva Vidal,
Technical University of Catalonia, Barcelona, Spain

In general, audio equalizers need second-order bandpass filters. Such cells require an easy and independent tuning of their parameters: the natural or central frequency, ω_0; the quality factor, Q; and the maximum bandpass gain, k. The use of cells with independent adjustments could require state-variable topologies. Unfortunately, this sort of structure usually needs at least three operational amplifiers. The basis for an alternative uses SAB (single-amplifier-biquadratic) filters. These cells allow obtaining second-order bandpass filters, but they have two main drawbacks: The quality factors that you can obtain with these cells have a practical maximum limit, and you cannot independently tune the three characteristic parameters.

This Design Idea instead uses the TQE (transimpedance-Q-enhancement) structure in an audio-equalizer (**Figure 1**). This cell has two advantages when you use it in equalizer circuits: You can adjust the three characteristic parameters in an independent way, but it uses only two operational amplifiers per cell. **Reference 1** presents the generic TQE topology. **Figure 1** shows the configuration that implements a bandpass filter based on the generic structure. This structure, which processes current-input signals, shows low-impedance input without the resistor R_{IN}. Considering that R_1 and R_3 are equal in value and that all the capacitors are equal to C, the transimpedance, Z(s), is:

$$Z(s)=\frac{V_{BP}(s)}{I_{IN}(s)}=\frac{R_1^2C_s}{R_1^2C^2s^2+(2-R_1/R_2)R_1Cs+1}.$$

However, by adding R_{IN}, the input has high impedance, allowing the processing of voltage input signals because R_{IN} provides the required voltage-to-current conversion. In this way, the input-to-output transfer function, H(s), is:

$$H(s)=\frac{V_{BP}(s)}{V_I(s)}=\frac{R_1}{R_{IN}}\frac{s/R_1C}{s^2+s(2-R_1/R_2)/R_1C+1/R_1^2C^2}.$$

Thus, the circuit implements a second-order bandpass-transfer function; the following **equations** yield the central frequency, ω_0, and the quality factor, Q:

$$\omega_0=1/R_1C;\ Q=\frac{R_2}{2R_2-R_1},$$

and the value of the gain, k, is:

$$k=\frac{R_1}{R_{IN}}Q=\frac{R_1}{R_{IN}}\left(\frac{R_2}{2R_2-R_1}\right).$$

Thus, you can make the adjustments of ω_0, Q, and k with R_1, R_2, and R_{IN}, respectively.

You can use the bandpass cell in **Figure 1** in an audio equalizer. **Figure 2** shows a possible implementation of a

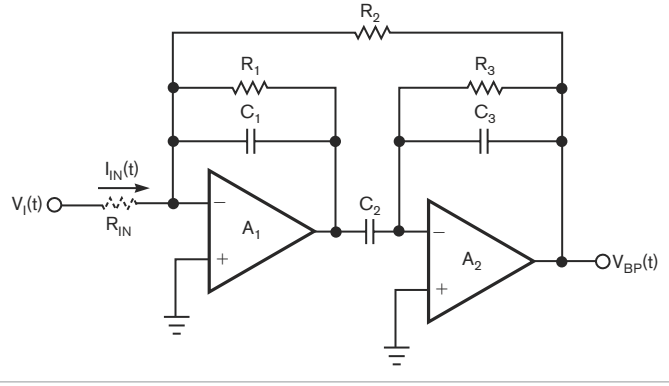

Figure 1 Adding R_{IN} to this bandpass filter based on a TQE structure causes the circuit to show high input impedance.

DIs Inside

66 AMI-to-NRZI-direct-conversion circuit tolerates unequalized pulse tails

70 Virtual RF generator measures load impedance and power

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graphic equalizer. The basis for the circuit is a bank of bandpass TQE cells. Note that the cells are TQE with low-impedance input. Thus, the input network's R_{IN} converts $V_{IN}(t)$ and $V_{OUT}(t)$ to the corresponding input current, $I_{IN}(t)$. Adjusting potentiometer R_{IN} with its wiper to the far left ($X_I \rightarrow 0$) accentuates the frequency band that the corresponding cell covers in the overall circuit output. On the other hand, positioning the wiper of R_{IN} to the far right ($X_I \rightarrow 1$) causes a large amount of negative feedback to occur at this same frequency, thus causing attenuation in the forward-signal path. In each case, the remaining filters' TQE_I receives percentages of both the input signal, $V_{IN}(t)$, and the output signal, $V_{OUT}(t)$, in ratios that their respective potentiometer settings determine.

You can derive the overall transfer function from **Figure 2**. The output voltage, $V_{OUT}(s)$, of the equalizer is:

$$V_{OUT}(s) = -\left\{V_{IN}(s) + A\sum_{I=1}^{N} Z_I(s)\left[\frac{V_{IN}(s)}{X_I R_{IN}} + \frac{V_{OUT}(s)}{(1-X_I)R_{IN}}\right]\right\},$$

where $Z_I(s)$ are the cells' transimpedances, and

$$A = \frac{R_B}{R_A}.$$

If you define

$$H_I(s) = Z_I(s)/R_{IN},$$

then the transfer function of the equalizer becomes

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = -\frac{1 + A\sum_{I=1}^{N}\frac{H_I(s)}{X_I}}{1 + A\sum_{I=1}^{N}\frac{H_I(s)}{1-X_I}}.$$

Now, you can investigate the effect of various settings of the potentiometers. For example, in the case with all of the controls centered, X_I equals 0.5 for each band. Then, $V_{OUT}(s)/V_{IN}(s) = -1$, as you would expect in a typical equalizer's response. Setting band I=1 to a value of X_I and all other bands flat—that is, $X_I = 0.5$ for I=2, 3, ... n), you obtain:

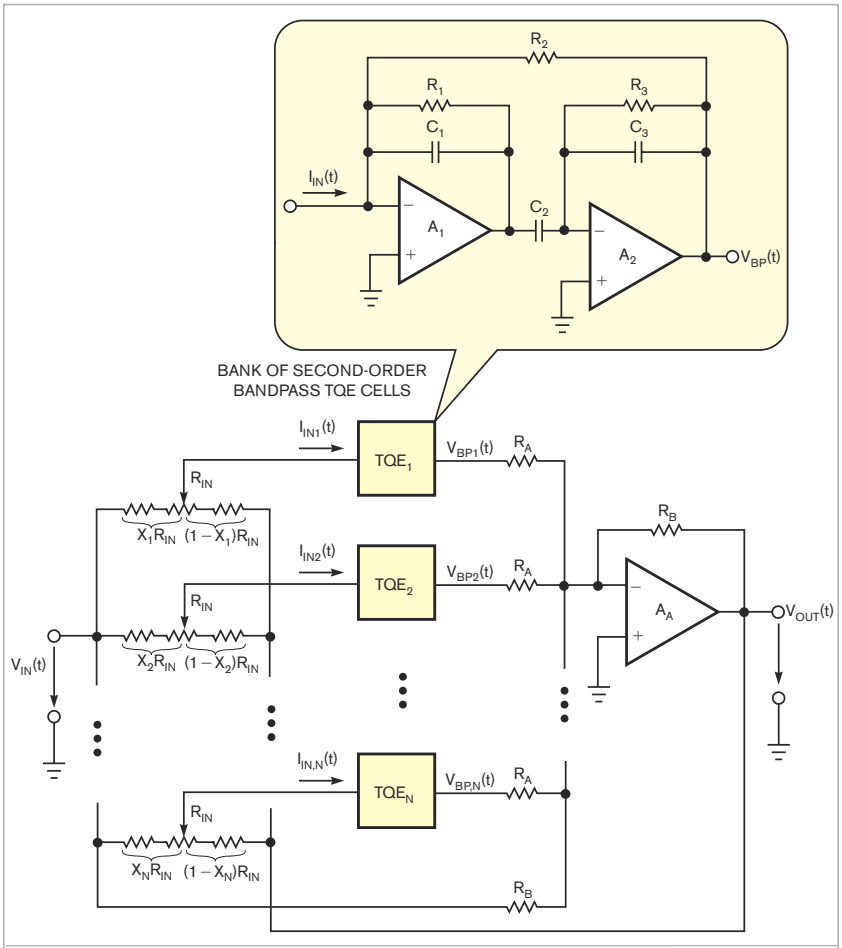

Figure 2 The TQE cells in this graphic equalizer have low-impedance inputs.

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{s^2 + \left(\frac{\omega_{01}}{Q_1}\right)\left[1 + \frac{1}{1+2AM}\left(\frac{A}{X_1} - 2A\right)k\right]s + \omega_{01}^2}{s^2 + \left(\frac{\omega_{01}}{Q_1}\right)\left[1 + \frac{1}{1+2AM}\left(\frac{A}{1-X_1} - 2A\right)k\right]s + \omega_{01}^2},$$

which represents a bandpass filter with unity gain, or 0 dB, in the stopband and a gain of A_O at resonance, and M is a constant representing the average value of the complete summation. M is approximately 1.3, or approximately 2.3 dB (**Reference 2**). Note that this gain can be higher—that is, boost—or lower than one. Considering as typical values M=1.3, A=1, and k=1, you can simplify the **equation** for passband gain A_O, which is equal to the ratio of the s term coefficients, as:

$$A_O = \frac{3.6 + \left(\frac{1-2X_1}{X_1}\right)}{3.6 + \left[\frac{1-2(1-X_1)}{1-X_1}\right]}.$$

As an example, consider the case of an octave-band equalizer with 10 bands. In this case, the value of the quality factor for each band is about 1.42 (**Reference 3**), and the typical central frequencies of the 10 sections are 32 Hz to 16 kHz. Adjusting R_{IN} in the input of the cell TQE with its wiper to the left boosts the frequency band that the corresponding cell covers in the overall circuit output. For instance, if X_I is 0.1, then A_O is approximately 13 dB. On the other hand, positioning the wiper of R_{IN} to the right causes attenuation in the forward-signal path. So, if X_I is 0.9, then A_O is

LINEAR TECHNOLOGY

DESIGN NOTES

Tiny Dual Full-Bridge Piezo Motor Driver Operates from Low Input Voltage – Design Note 436

Wei Gu

Introduction

Piezoelectric motors are used in digital cameras for autofocus, zooming and optical image stabilization. They are relatively small, lightweight and efficient, but they also require a complicated driving scheme. Traditionally, this challenge has been met with the use of separate circuits, including a step-up converter and an oversized generic full-bridge drive IC. The resulting high component count and large board space are especially problematic in the design of cameras for ever shrinking cell phones. The LT®3572 solves these problems by combining a step-up regulator and a dual full-bridge driver in a 4mm × 4mm QFN package. Figure 1 shows a typical LT3572 Piezo motor drive circuit. A step-up converter is used to generate 30V from a low voltage power source such as a Li-Ion battery or any input power source within the part's wide input voltage range of 2.7V to 10V. The high output voltage of the step-up converter, adjustable up to 40V, is available for the drivers at the V_{OUT} pin. The drivers operate in a full-bridge fashion, where the OUTA and OUTB pins are the same polarity as the PWMA and PWMB pins, respectively, and the $\overline{OUTA}$ and $\overline{OUTB}$ pins are inverted from PWMA and PWMB, respectively. The step-up converter and both Piezo drivers have their own shutdown control. Figure 2 shows a typical layout .

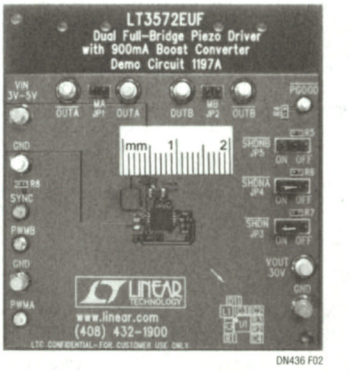

Figure 2. Typical Layout for the Figure 1 Converter

Single Driver Application

Each full-bridge Piezo driver can be independently enabled and disabled by controlling the $\overline{SHDNA}$ and $\overline{SHDNB}$ pins. When held below 0.3V, $\overline{SHDNA}$ and $\overline{SHDNB}$ prevent the drivers from switching and keep the outputs in a high impedance state.

In applications where only one driver is used, the unused driver can be simply turned off without wasting any power by tying either $\overline{SHDNA}$ or $\overline{SHDNB}$ pin to the GND. Figure 3 shows a typical single driver application circuit where only driver A is enabled. The input pin PWMB is tied to GND.

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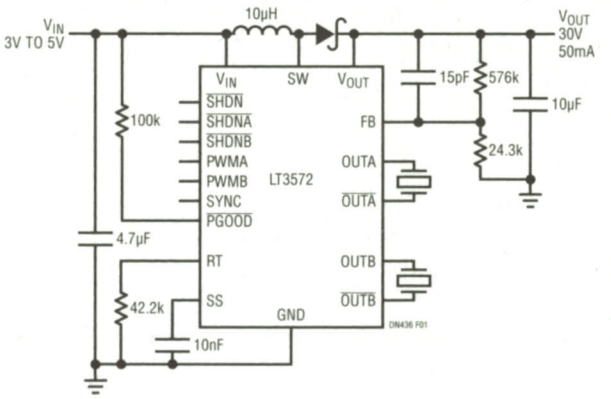

Figure 1. Typical Circuit

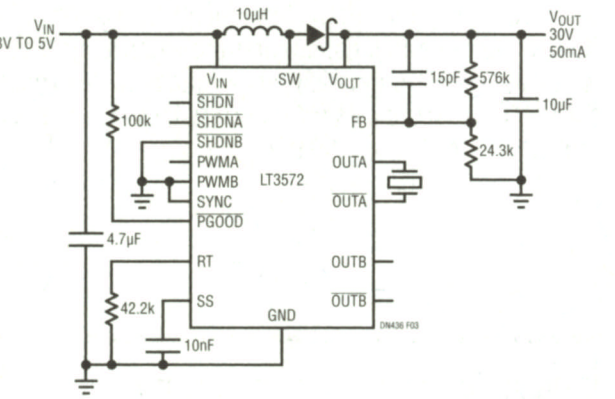

Figure 3. Single Driver Application Circuit

Using External Power Supply

The high output voltage of the step-up converter, adjustable up to 40V, is available for the drivers at the V_{OUT} pin. For some multiple Piezo motor applications with multiple LT3572s, all the full-bridge drivers are powered by an external high voltage power supply. In this case, the integrated step-up converter can be simply disabled and only the dual drivers are used. In Figure 4, the $\overline{SHDN}$ pin is tied to the ground so the step-up regulator is prevented from switching. The SW pin, RT pin, SS pin and $\overline{PGOOD}$ pin are left open. The V_{IN} pin should be connected to a voltage source between 2.7V and 10V and FB pin to any voltage between 1.3V and 3V. In this example, the V_{IN} pin and FB pin are connected together, and both drivers are fully functional while the step-up converter is not running. The V_{IN} current is normally below 10mA.

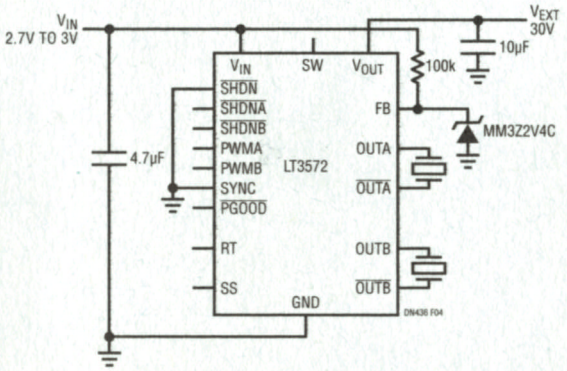

Figure 4. Using External Power Supply with Integrated Step-Up Converter Disabled

Operating Piezo Motor with Long Wires

In some cases, the Piezo motors are physically located far away from the driver. The parasitic inductance of the long connecting wires and capacitive Piezo motor form a high Q resonant LC tank. If the oscillation is not properly dampened, the driver pins would see large negative voltages, possibly causing spurious operation of the IC. Schottky diodes can be added at the OUTA and OUTB pins to prevent ICs from seeing large negative voltage. Another way to solve this problem is to add a resistor between the driver and the Piezo motor, as shown in Figure 5, to slow down the driving speed and dampen the oscillation. In this example, the connecting wires are 1-foot long twisted wires and the resistor is 20Ω. The voltage waveforms of the $\overline{OUTB}$ pin are shown in Figure 6 without the resistor, and Figure 7 with the resistor.

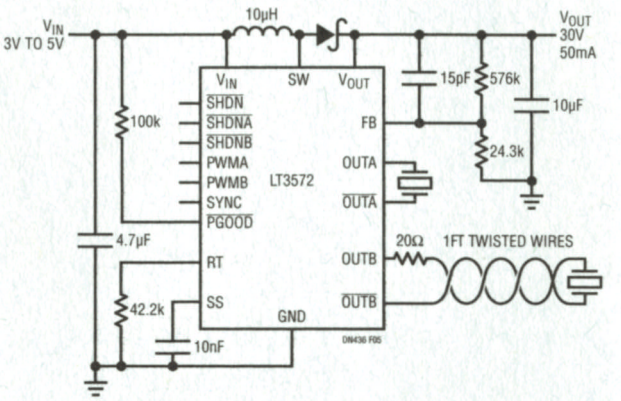

Figure 5. Adding a Resistor when Operating with Long Wires

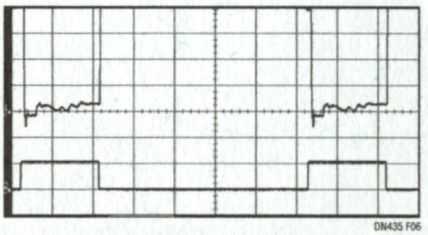

Figure 6. $\overline{OUTB}$ Voltage Without the Resistor. Top Trace: $\overline{OUTB}$ Voltage (2V/Div), Bottom Trace: PWMB Voltage (2V/Div)

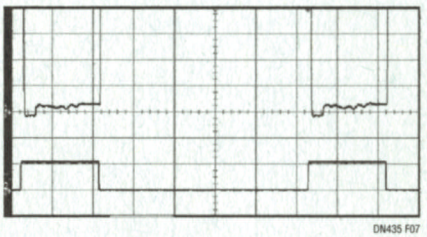

Figure 7. $\overline{OUTB}$ Voltage with the Resistor. Top Trace: $\overline{OUTB}$ Voltage (2V/Div), Bottom Trace: PWMB Voltage (2V/Div)

Conclusion

The LT3572 is a complete Piezo motor drive solution with a built-in high efficiency internal switch and integrated dual full-bridge drivers. Its fixed frequency, soft-start function, internal compensation and small footprint make the LT3572 a very simple and small solution to drive Piezo motors.

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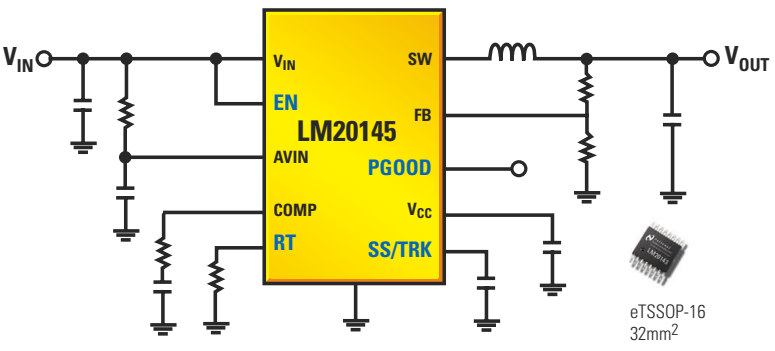
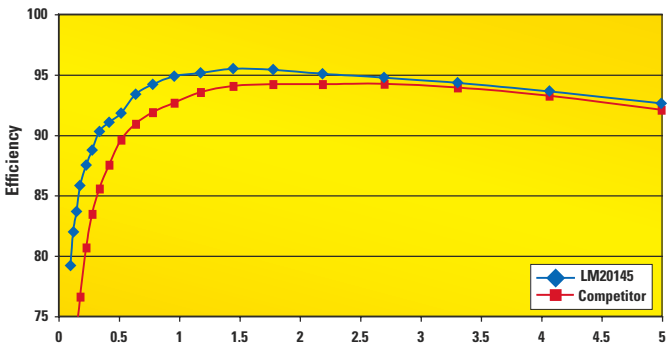


Efficiency vs Output Current (V_{IN} = 5.0V, V_{OUT} = 3.3V, fSW = 500 kHz)



Product Number	V_{IN} (V)	I_{OUT}	SYNC IN	Frequency Adjust	SYNC OUT	Frequency
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LM20133	2.95 to 5.5	3	✔			Sync
LM20143	2.95 to 5.5	3		✔		500 kHz - 1.5 MHz
LM20124	2.95 to 5.5	4				1 MHz
LM20134	2.95 to 5.5	4	✔			Sync
LM20144	2.95 to 5.5	4		✔		500 kHz - 1.5 MHz
LM20154	2.95 to 5.5	4			✔	1 MHz
LM20125	2.95 to 5.5	5				500 kHz
LM20145	2.95 to 5.5	5		✔		250 kHz - 750 kHz
LM20242	4.5 to 36	2		✔		250 kHz - 750 kHz

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approximately −13 dB. You must have a minimum input impedance in each cell for the input voltage, $V_{IN}(t)$, and the feedback voltage, $V_{OUT}(t)$. Thus, the inclusion of two resistors in series with each potentiometer R_{IN} in **Figure 2** guarantees this resistance. EDN

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AMI-to-NRZI-direct-conversion circuit tolerates unequalized pulse tails

Glen Chenier, TeeterTotterTreeStuff, Allen, TX

AMI (alternate-mark inversion) is a three-level—positive, zero, negative—copper-cable transmission code with the useful property of having no dc component for ease of ac coupling using capacitors or line-coupling transformers and a spectral peak at one-half the symbol rate. The zeros symbols transmit as 0V; the ones symbols transmit at half-unit intervals with alternating-line polarity to maintain the dc balance.

An interesting feature of the three-level AMI code is that you can easily translate it directly from and to the two-level NRZI (non-return-to-zero-inverted) code. The basis for NRZI is a transition, not a level; an NRZI edge in either the rising or the falling direction signifies a logic one. A lack of transition in a given symbol interval signifies a logic zero. Thus, the NRZI code is invertible without destroying the logic sense. Absolute level is meaningless. The only information content is the change or no change of level at the expected transition time. Likewise, the AMI code is invertible; you need not worry about the twisted-pair polarity. **Figure 1** shows the relationships between NRZ (non-return-to-zero), NRZI, and AMI codes.

The usual received-data-recovery method for AMI comprises a pair of voltage-level slicers, or comparators, that combine the transmission-line-positive and -negative marking symbols into a two-level RZ code (**Figure 2a** through **d**). The symbols are then further changed into the standard NRZ-logic representation (not shown), typically with a D-type sampling flip-flop or similar circuitry.

One impediment to successful AMI transmission over distance is the "pulse-tail"-cable artifact. When you do not drive the cable to a positive- or a negative-marking pulse, such as in a zero following a one, the last transmitted marking pulse extends in time and slowly decays to zero. This effect becomes more pronounced as the cable gets longer, and, unless you eliminate it through the use of a frequency-equalization network that matches the cable-length and -attenuation characteristics, it will wreak havoc on the data-recovery slicers (**Figure 2e** and **f**).

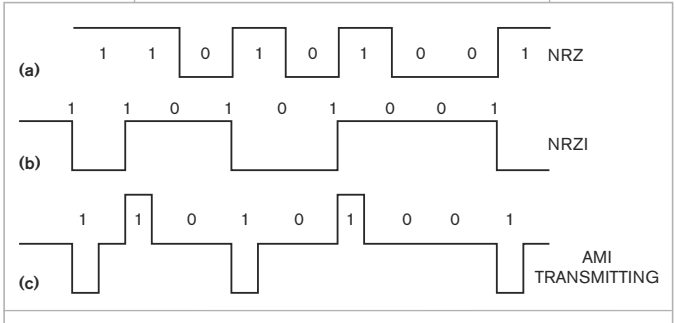

Figure 1 These waveforms illustrate an NRZ-to-NRZI-to-AMI conversion. Only when NRZ (a) is at logic one does NRZI (b) change at bit boundaries. AMI marks at the polarity of the NRZI transition (c).

You can easily convert two-level NRZI to three-level AMI through a straightforward algorithm that you can implement with a few gates and line drivers, a transformer, and a delay line if the system clock is unavailable. If no NRZI transition exists, transmit nothing for that symbol interval. For every rising NRZI edge, transmit a marking pulse, usually with a duration of one-half-symbol interval. For convenience, assign this pulse polarity as positive. For every falling NRZI edge, transmit a similar marking pulse of the opposite polarity to that of the rising edge. This step automatically creates the alternate marking polarities. Again for convenience, assign this pulse polarity as negative.

Recovering the NRZI directly from the AMI is likewise a straightforward algorithm (**Figure 3a** and **b**). If there is no received-voltage-threshold crossing of opposite polarity to that of the previous marking-threshold crossing, retain the last received-marking state at logic high or logic low. If the received-AMI voltage crosses a threshold at a polarity opposite to the current state of the detector output, toggle the detector output to the state associated with that new polarity. Again, for convenience, if the AMI-pulse-threshold crossing is positive above the midlevel, or zero, toggle the detector output to a rising edge; if the AMI-pulse-threshold crossing is negative below the midlevel, or zero, toggle the detector output to a falling edge.

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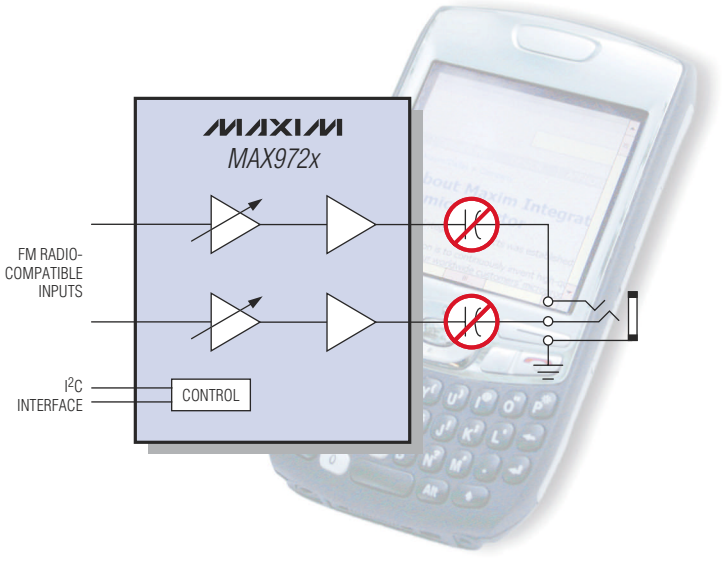

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MAX9726	Headphone amp with bass boost, 64-step volume control	2.7 to 5.5	20-UCSP (2 x 2.5), 20-TQFN (4 x 4)
MAX9729	Headphone amp with bass boost, 32-step volume control, input mux	1.8 to 3.6	28-TQFN (5 x 5)

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From these algorithms, you can see that this receiving method directly translates the AMI code into the NRZI code. Also, by its requirement for alternate marks to cross the zero level and the subsequent opposite threshold to cause an output toggle, this method is immune to the marking-pulse tails that poorly or nonequalized lengths of transmission line cause (**Figure 3c** and **d**). This effect gives rise to the possibility of eliminating the amplitude/frequency-equalizer portion of the receiver for high-bit-rate data transmission on medium-length copper cables.

A circuit that fulfills the receiver algorithm is a Schmitt trigger with an upper trip point and a lower trip point that are above and below the midlevel of the AMI three-level signal. You can easily set this point as a hardware bias with ac coupling of the dc-balanced AMI signal because there is virtually no baseline wander with AMI (**Figure 4**). Gain and drive level are not critical as long as sufficient pulse amplitude exists to cross the trip thresholds. If the signal is excessively strong or the trip thresholds are close to the midsignal level, the circuit still correctly translates data as long as no end-of-pulse ringing crossing into the opposite trip thresholds occurs. If this scenario occurs, pulse tails are beneficial, and you can artificially introduce them for the minimum operational cable length if necessary. For some oscilloscope-photo waveforms using the ECL Schmitt trigger of **Figure 4**, go to www.edn.com/080306di.EDN

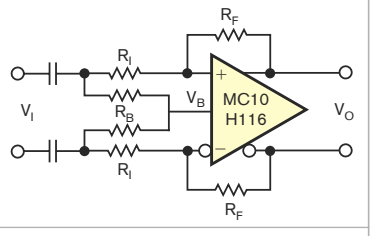

Figure 4 An MC10 H116 configured as a Schmitt-trigger circuit uses an ECL-amplifier stage. R_F supplies the positive feedback; the ratios of R_F to R_I set the hysteresis and thus the upper- and lower-trip-point-voltage levels. To remain within the linear region of the MC10 H116 transfer function, ±100 to 200 mV from center zero level is suggested.

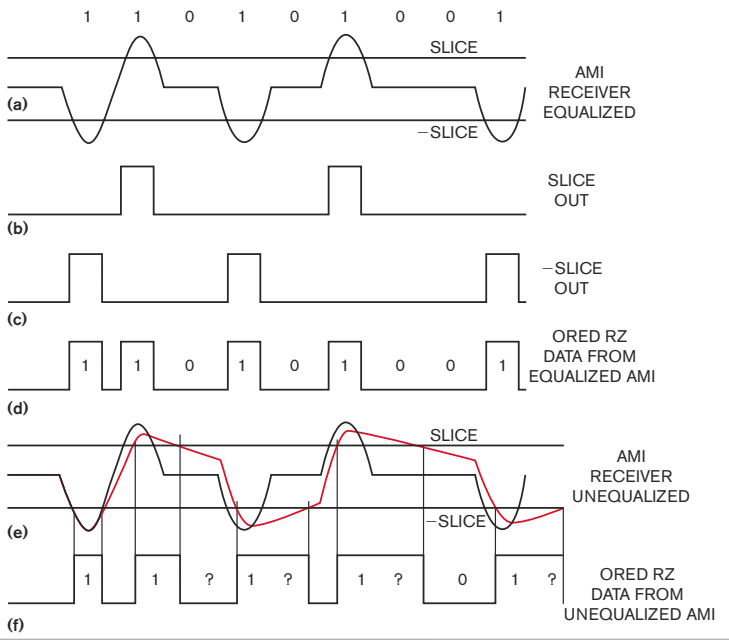

Figure 2 These waveforms show the usual transcoding of AMI to RZ. Two digital comparators slice bandlimited, equalized AMI (a). ORing the comparators, one for positive polarity (b) and one for negative polarity (c) produces RZ data (d). The digital comparators may themselves be Schmitt triggers for clean switching and immunity to small noise levels riding on the analog AMI. Unequalized AMI, superimposed on equalized AMI (e) causes the marking pulse tails, resulting in a highly distorted and error-filled RZ data waveform (f).

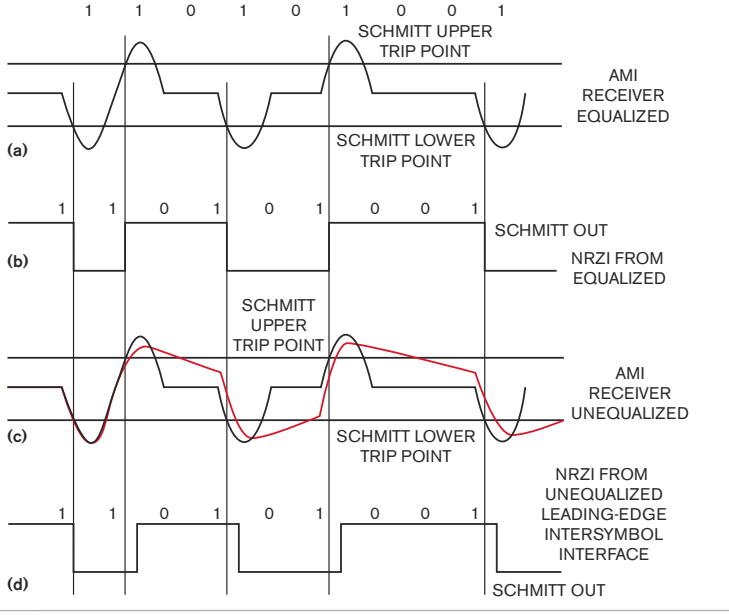

Figure 3 A Schmitt trigger directly converts bandlimited, equalized AMI (a) into the original NRZI (b). Once AMI crosses a trip point, no further transition at Schmitt output (c) is possible until the AMI crosses the opposite trip point. Unequalized AMI, superimposed on equalized AMI, cause marking pulse tails, resulting in little waveform distortion (d). Some data-dependent timing jitter occurs because of leading-edge intersymbol interference.

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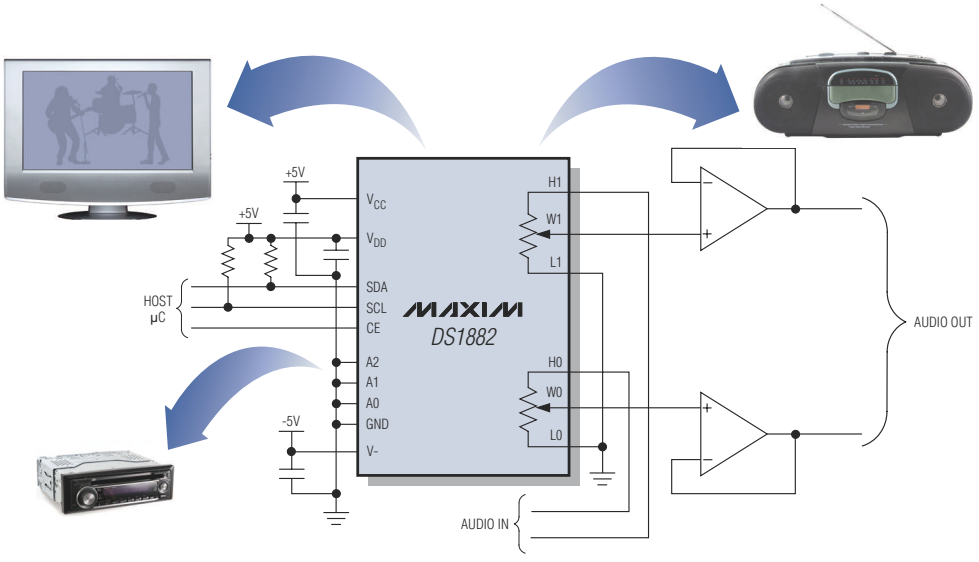

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Virtual RF generator measures load impedance and power

Michael Nasab, Circuit Mentor, Boulder Creek, CA

Calculating the load impedance and power consumption at high frequencies in RF circuits is a tedious task. This Design Idea describes a VI (virtual instrument) that provides an easy way to quickly and effectively measure these parameters. You can measure and display the power and impedance of various types of loads, such as resistive or series/parallel tank circuits, at any given frequency. Using National Instruments (www.ni.com) LabView, you can easily modify the VI to accommodate any type of load having any complexity. The virtual RF generator comprises power-supply, amplifier, and load-select/measurement-display modules.

The amplifier module, with as much as 90% efficiency, provides frequencies of 100 kHz to 1 MHz with adjustable ac power applied to the load. The load-select-and-display module provides a sine or square waveform, load-selection type, and adjustment.

Figure 1 shows the VI driving a resistive load. Adjusting the frequency from minimum to maximum has no effect on the output impedance and power. You can download the VI and watch a flash movie describing three examples at www.circuitmentor.com.EDN

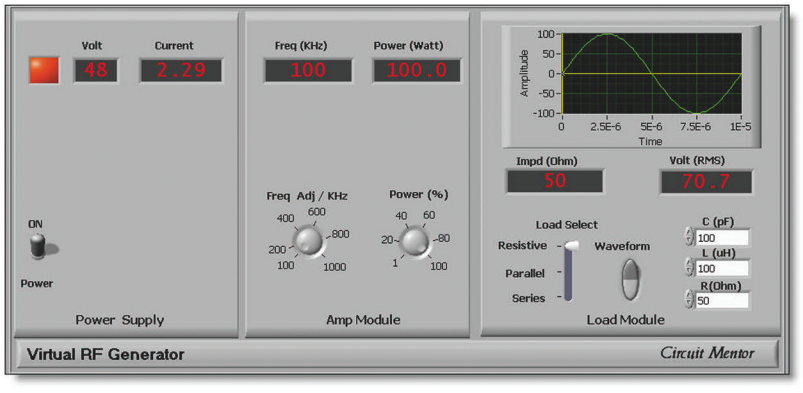

Figure 1 These settings on the virtual instrument measure the impedance and power of a resistive load.

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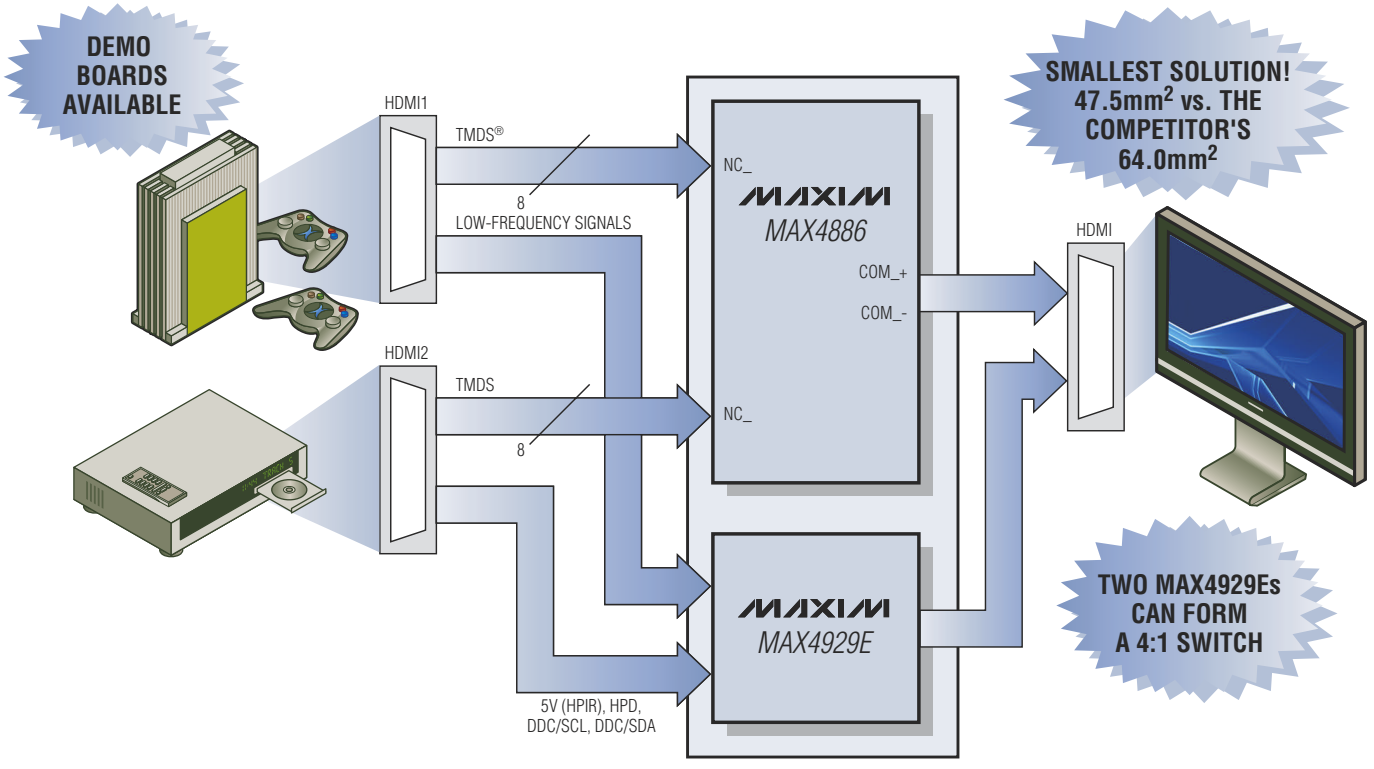

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LINKING DESIGN AND RESOURCES

Demand grows for distributor-demand creation

Demand creation—the use of price reductions or other incentives to create or increase immediate sales response for a product or service among consumers or resellers—is a growing aspect of the distribution business, according to Harley Feldberg (**photo**), president of Avnet Electronics Marketing (http://em.avnet.com), an operating group of Avnet (www.avnet.com) Inc. The executive notes that, over the last two years, suppliers have been embracing distribution for demand creation, offering more attractive rewards, including bonuses for superior performance in demand creation.

Feldberg notes that, 10 or 15 years ago, there were a number of broad-line-semiconductor manufacturers. Feldberg says,

"Almost all of our key suppliers have gotten more focused on a select group of technologies. Because of that [focus], there is an opening for someone to fill the void of aggregating all of these technologies into … what we internally call a design chain. … That trend has been driving a need on our suppliers' behalf to rely more on the channel for demand creation, especially in the mass market."

Avnet in 2007 promoted one of its latest demand-creation wins: Maxim Integrated Products. The agreement marked a change in the analog-, linear-, and mixed-signal-semiconductor maker's business model—Maxim declined to use the distribution channel for demand creation for 25 years. "Maxim is one of a few large semiconductor guys that hasn't embraced the channel," Feldberg says. "There probably aren't a lot of commodities that are better suited for distribution in general than analog [products]. … In many ways, it's a custom product."

Feldberg estimates that, of Avnet's total business, approximately 35% currently comes from demand creation. He says the electronics-supply-chain giant's "loose goal" over time is for 50% of its business to be demand-creation-like, with the remaining half coming from fulfillment.

GREEN UPDATE

ONTARIO BEGINS WEEE DIRECTIVE COMPLIANCE

Ontario, Canada, is implementing its own version of the WEEE (waste-electrical-and-electronic equipment) directive for the recycling, reuse, and refurbishment of certain electronics. The Ontario Electronic Stewardship (www.ontarioelectronicstewardship.ca) backs the plan, which should impact electronics design, just as previous versions of WEEE have in the European Union and Asia-Pacific countries. The plan follows Ontario's Waste Diversion Act and Regulation 393/04, which designates a list of electronic equipment that requires waste-diversion programs.

The directive proposes to establish an industry-led, provincewide waste-diversion program for electronic equipment in two phases. The first phase will cover computers and accessories, computer monitors, printers, fax machines, and televisions. The second phase will add PDAs, copiers, flatbed scanners, land-line and cell phones, and audio-visual equipment. The Ontario Electronic Stewardship is moving to Phase One, with Phase Two implementation expected thereafter.

Like the previous countries that have launched a WEEE directive, Canada is initiating WEEE to reduce its waste, as well as keep hazardous chemicals out of landfills. The country has also recognized the reuse of resources such as ferrous metals, aluminum, and copper, which electronics often contain. Ontario joins several other Canadian provinces, including Alberta, Nova Scotia, and Saskatchewan, in taking WEEE action.

OUTLOOK

APPLICATION PROCESSORS FACE FALLING UNIT PRICES

Although application processors are increasingly important enablers of multimedia capabilities in high-end smartphones and feature phones, this market will face challenges over the next several years, according to ABI Research (www.abiresearch.com). The company expects that, from 2007 to 2012, dropping unit prices will offset strong unit growth, according to ABI Senior Analyst Doug McEuen. "After significant increases during the next two years, the decline in unit prices will compress the application-processor revenue to a flat growth rate," he says.

Obstacles to application-processor-unit shipment growth include integration and the emergence of ultralow-cost handsets.

ABI Research estimates that application-processor revenue will reach nearly $2.8 billion by 2012, with unit shipments of 553 million at a cost of $5.04 per unit. Despite an expected decline in smartphone revenue from $3.3 billion in 2007 to $2.1 billion in 2012, the company projects that the smartphone segment will be the largest market for application-processor-unit shipments in the five-year period. High-end feature-phone unit shipments are expected to increase by 42%, and revenue will rise by almost 21%, McEuen says.

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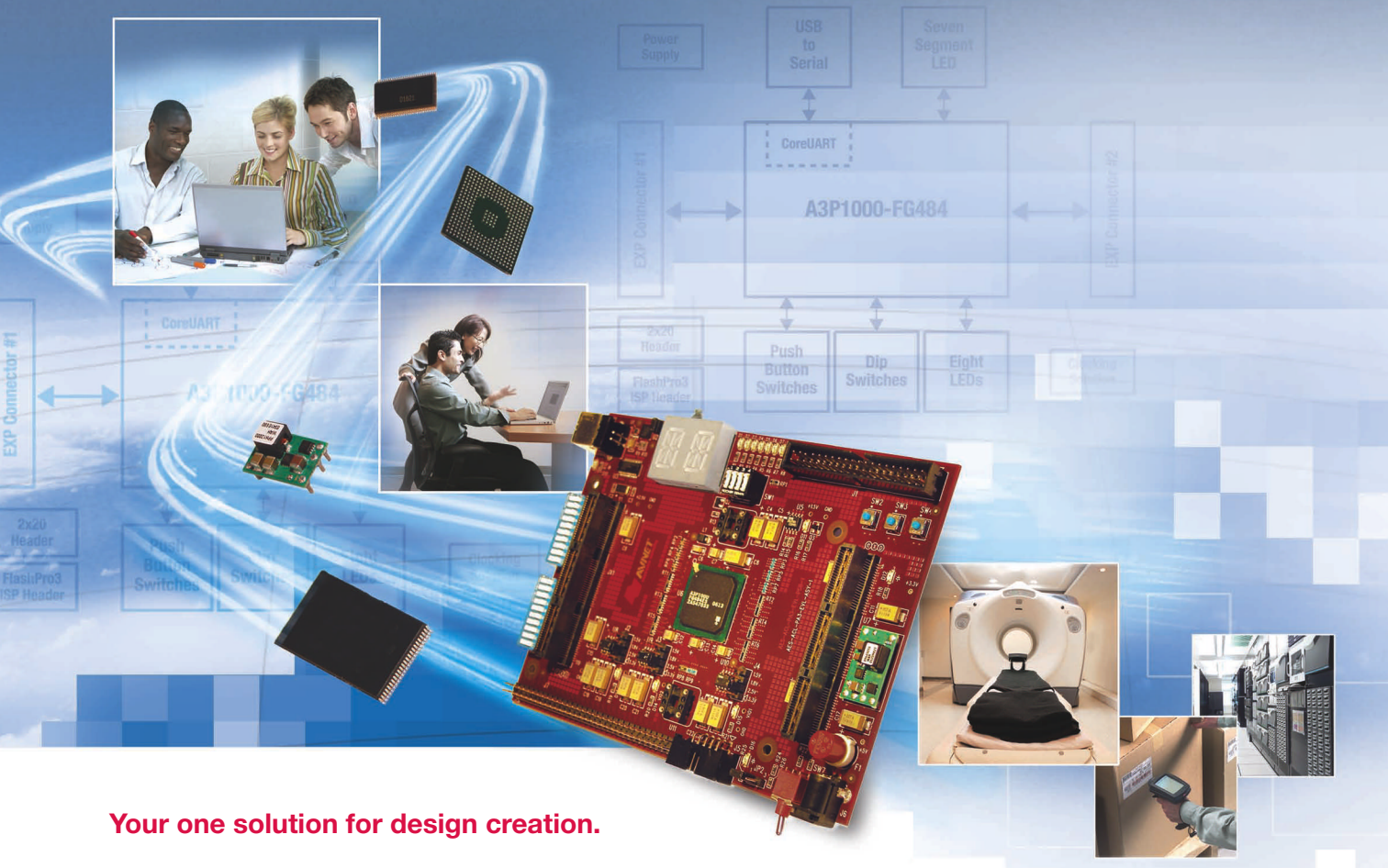

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POWER SOURCES

Rectifier module provides 2000W of power

With a typical power-conversion efficiency of 96%, the Flatpack2 HE rectifier module suits use in telecommunications applications. The 48/2000 ac/dc power rectifier provides a stand-alone 48V rectifier and a battery charger providing 2000W of power. Features include a CAN (controller-area-network)-bus interface, an 85 to 300V-ac input-voltage range, and a 41.7A maximum output current. Protection capabilities include overvoltage shutdown, a blocking diode, short-circuit and high-temperature protection, and a front-to-back airflow with chassis-integrated heat sinks. The Flatpack2 HE rectifier module costs $450.

Eltek Valere, www.eltekvalere.com

Power adapter provides 84% efficiency

Targeting worldwide use, the AD80 ac/dc power adapter features a universal 90 to 264V-ac input voltage and produces one regulated 24V output voltage capable of 3.25A continuous delivery. The adapter complies with the One Watt Input Energy Star/Blue Angel requirement and provides 84% typical efficiency. The adapters include comprehensive protection against, including automatic recovery from, overvoltage, overcurrent, and overpower conditions and have a 300,000-hour MTBF (mean-time-between-failures) rate at a full load and 25°C ambient temperature. Providing a 0 to 40°C operating temperature without derating, the AD80 ac/dc power adapter costs $45.

Emerson Network Power, www.powerconversion.com

Wall-mount rectifier system provides a range of output voltages

The wall-mount RF series of rectifiers operates stand-alone or in parallel, providing redundancy or higher output ratings. The rectifier system functions as an alternative to rack-mount units for powering a variety of telecom equipment. Features include a 290 to 700W output-power range with 12, 24, and 48V output voltages; a 100 to 275V-ac input range for output power; and active power-factor correction. Prices for the RW series of convection-cooled units range from $520 to $620.

Unipower Telecom, www.unipower-corp.com

POL converters power DDR 1, DDR2, and DDR3 memory

Claiming 88% efficiency, the 60A VCN60BADJTU-1C and 70A VCN70BADJTU-1C POL (point-of-load) dc/dc converters provide a 50A/in.^{3} current density. The converters feature a programmable 0.6 to 3.5V output-voltage range with 0.5% typical setpoint accuracy, 12V-dc input voltage, and a standard 1U module height. High-current densities allow powering of DDR1, DDR2, and DDR3 memory, as well as general-purpose ICs in multiple applications. Additional features include a soft-start circuit, differential remote sensing, power-good signal, prebias turn-on, and output enable. The 60 and 70A versions measure 61×9.5×31.8 and 61×16.8×31.8 mm, respectively and cost $23.10.

Murata Power Solutions, www.murata-ps.com

Switchers provide autoranging from 90 to 264V-ac input

Providing 250W of output power in a U chassis, the MPA250X ac/dc-switcher series includes an autoranging 90 to 264V-ac input and power-factor correction. The 10 models operate over a 90 to 132 or 180 to 264V-ac autoranging input, allowing tightly regulated single outputs. Factory-set, user-adjustable outputs are 5, 9, 12, 15, 18, 24, 28, 36, 48, or 54V dc. Features include

productroundup

POWER SOURCES

a power-factor correction to EN61000-3-2 A, FCC class B emissions, 3000V-ac I/O isolation, and a 20-msec holdup time. Available in a 5×3.2×1.5-in. 1U chassis, members of the MPA250X family cost $75.40 each.

MicroPower Direct, www.micropowerdirect.com

1000 and 1500W power supplies operate in explosive-gas atmospheres

Adding to the vendor's 500W LZ-Sa series of industrial power supplies, the 1000 and 1500W power supplies target industrial and commercial applications. Suiting harsh environments, the devices comply with military standard 810E for shock and vibration and operate in explosive-gas atmospheres. Available in 12V in 1000W or 24V in 1000 or 1500W, the power supplies feature 10 to 15.75V and 18 to 29.4V user-adjustable ranges, respectively. Integral fan-cooling provides full-rated output power from −40 to +60°C and derating linearity to a 60% load at a 71°C ambient temperature. Accepted input ranges include 85 to 265V ac and 47 to 440 Hz, and the devices feature active power-factor and harmonic correction. The power supplies comply with SEMI-F47 standards for a 100V-ac input droop at full load and provide a 75-mV p-p output ripple and noise. Providing 20-msec holdup and ride-through allows the devices to avoid nuisance tripping during transient electrical interruptions. Available in 5.62×4.75×10.5-in. packages, the LZSa1000 and LZSa1500 cost $825 and $1250 (100), respectively.

Lambda, www.lambdapower.com

INTEGRATED CIRCUITS

ADC features 1M samples/sec and 16 input channels

Providing 1M-sample/sec conversion speed using 2.4 mA suits the AS1542 multichannel successive-approximation ADC for networking equipment, motor control, industrial automation, wired and wireless communications, and other forms of data acquisition. Providing 12-bit resolution on each of the 16 input channels, the channels are software-configurable as 16-channel single-ended or eight-channel fully-differential analog inputs. Features include a 2.7 to 5.25V supply voltage, a −40 to +85°C temperature range, and a 0.5-µA supply current in automatic-shutdown mode. The converter includes an interface-drive-voltage function enabling a serial interface connecting to 3 or 5V processor systems independent of the ADC's supply voltage. A sequencer and channel counter allow continuous or single conversions on selected channels with no additional user input or interruption of conversions. The device can be interfaced using a high-speed SPI (serial-peripheral interface)/QSPI (queued-serial-peripheral interface)/Microwire or DSP (digital-signal-processing) interface. The AS1542 successive-approximation ADC costs $4.88 (1000).

austriamicrosystems, www.austriamicrosystems.com

16-channel analog switches target medical-ultrasound applications

Targeting medical- and nondestructive-testing applications, the high-voltage, 16-channel HV2631 and HV2731 analog switches provide high-resolution imaging for medical-ultrasound-diagnostic-imaging equipment. The units are available as two sets of eight SPST (single-pole/single-throw) analog switches; both ICs' outputs provide a 22Ω typical on-resistance. The HV2731 features integrated bleed resistors for discharging residual dc voltages and reducing erroneous signals. All parts comply with "green" and ROHS (restriction-of-hazardous-substances) initiatives. Available in LQFP-48 packages, the HV2631FG-G and HV2731-FG-G cost $14.75 and $14.95 (1000), respectively.

Supertex, www.supertex.com

Powerline-communications chip set has a 100-Mbps maximum data rate

Comprising the DSS8101 PHY (physical)/MAC (media-access-control)-layer chip and the DSS7800 AFE (analog front end) chip, the Montgo powerline-communications chip set provides a 100-Mbps maximum data rate. The chip set offers full interoperability with the vendor's UPA-DHS (Universal Powerline Association/Digital Home Systems Standard)-compliant 200-Mbps products and future 400-Mbps powerline products. The Montgo powerline-communications chip set costs $5.55.

DS2, www.ds2.com

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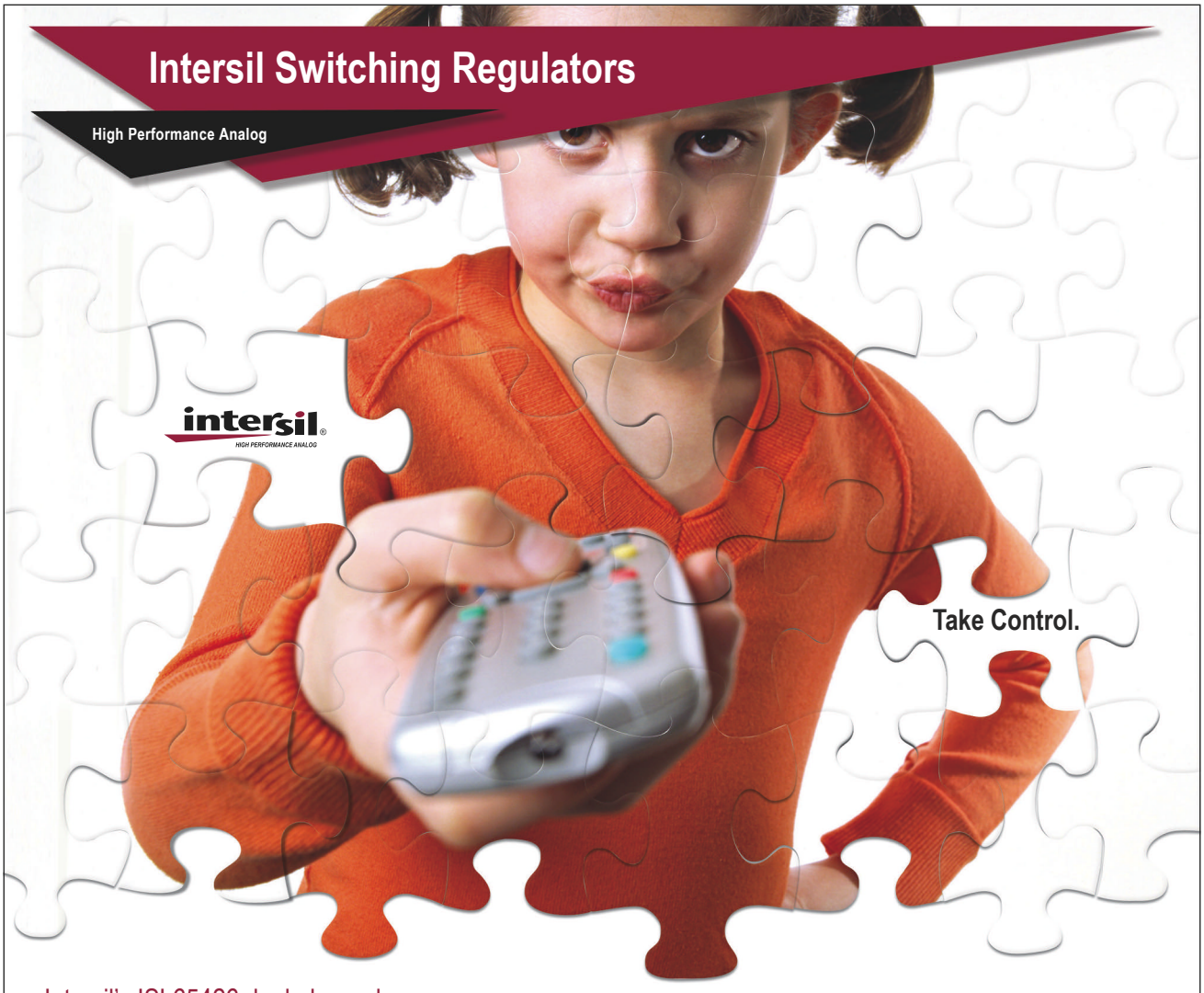

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0	1	5A	LX1, LX2, LX3, LX4, LX6	1A	LX5
0	0	2A	LX1, LX2, LX3, LX4, LX6	4A	LX3, LX4, LX5, LX6
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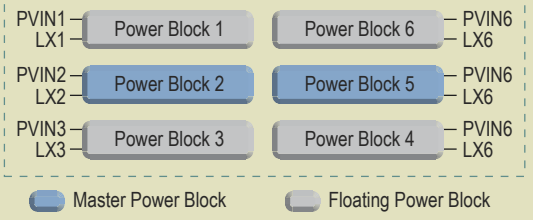

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BY WALTER LINDENBACH

Power, power everywhere but nary a watt to blink

DANIEL VASCONCELLOS

Oil fields—often miles in diameter—dot the farmland around Calgary, Alberta. Some fields contain more than 200 pumps. Although some people consider them picturesque, these pumps can produce an environmental disaster. The three-phase, 550V-ac electric motors that typically drive these machines pump thousands of gallons per minute of an oil-brine mixture through miles of pipe to the processing plant. If the processing plant fails, a reservoir stores the flow from the wells for eight hours. After that, pumping would cause the oil-brine mixture to flood the surrounding farmland. The only remedy would be to replace the land at astronomical cost. Turning off the power would stop the pumps but leave a large farming area in the dark. In winter, snow makes driving to the wells impossible.

An engineer at an oil company, Rick, had an idea: Interrupt power for 10 seconds, restore it for 20 seconds, and interrupt it again for 10 seconds. A sequence decoder at each well site could turn off the pumps until an operator manually restarted them. The power company's managers initially vetoed this approach. But when Rick described a scenario of oil fields at the ends of snowed-in roads producing oil and brine that had to go somewhere at −40°F, they quickly changed their minds.

The request for proposal specified a device that would operate on three-phase, 550V-ac power and continue operating during the power-interruption sequence; operate over −40 to +100°F; and detect a power-interruption sequence of 10 seconds off, 20 seconds on, 10 seconds off, and then on again indefinitely. The device would then leave the pump-motor contactors off until an operator manually reset them.

In those days, there were no supercapacitors, and capacitors with the required ratings were too large and too expensive. Batteries at this temperature range would unacceptably compromise reliability and increase maintenance costs. It occurred to me that the energy a capacitor stores is proportional to the square of the capacitor's voltage. So, with relatively small capacitance requirements and a little two-transistor regulator, we could charge the capacitor to 60V dc with a power resistor and one diode, and the regulator could provide 10V dc for longer than one minute.

Now, we had to consider how to control a 550V-ac contactor solenoid. When the device detected the power-off sequence, it had to turn off power until someone manually reset it. The peak value for 550V ac is approximately 780V, so, in the worst case, the control device would have to sustain 1000V peaks—and inductive spikes—not a job for a CMOS device! A magnetic circuit breaker and an SCR (silicon-controlled rectifier) would do it: When the SCR triggered, it would briefly apply 10V to the breaker coil, and the breaker would trip, opening the SCR and the motor-control contactor-solenoid circuits. The contactor would open and stay open until an operator reset the breaker. But we were still concerned about the 1000V peaks and inductive spikes on the circuit-breaker contacts. An engineer at circuit-breaker manufacturer ETA (www.e-t-a.com) told me that the breaker that I was considering would survive in this application.

After Rick awarded the contract, he told me that a competitor had phoned him for a clarification of the specifications. He asked, "How are we supposed to keep this thing going during the power-off periods? Should we use a battery?"

Rick replied, "No."

"Well then, what are we supposed to do?" he asked.

Rick replied, "Think!" EDN

Walter Lindenbach founded and operated Calgary Controls Ltd and is now retired. Share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

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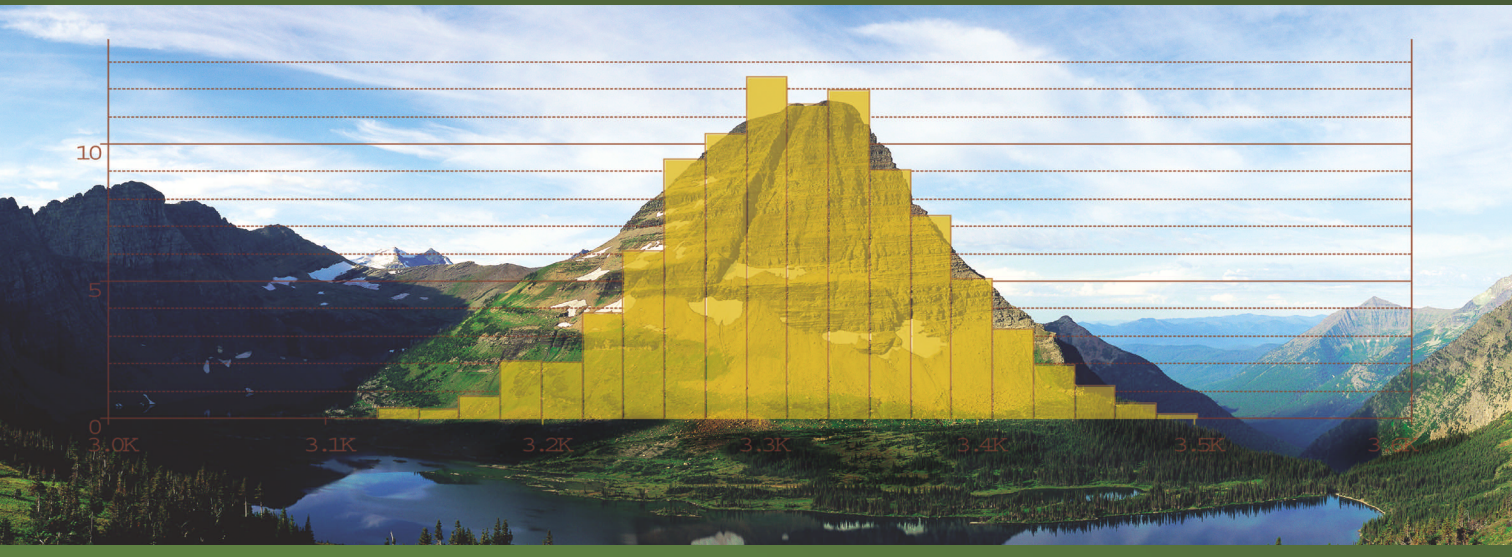

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